

# **Proximity Communication Interface Implementation Specifications**

**Version 1.1**

**JULY 2001**

**New Media Development Association**  
(foundational juridical person)

## Foreword

The New Media Development Association has developed a "Development of Platform for New Generation Smart Card Systems" based on an innovative architecture that is able to accommodate new functional requirements and diverse security levels with the aim of systematically integrating the various card specifications in existence at present as a part of the "Industrial and Social Information Infrastructure Development Project" implemented by the Japan Information Processing Development Corporation in accordance with the third supplementary budget for the 1998 fiscal year. This development was carried out with particular focus on contactless IC cards --- proximity cards (PICC) as defined in ISO/IEC 14443 for which popularity is expected to grow in a wide range of IC card applications in the future. The "Proximity Communications Interface Implementation Specification" (Version 1.0) were released in December 2000 in the form of a disclosed technical reference that summarized the results of studies for improving compatibility between PICC and proximity coupling devices (PCD) based on experience acquired during the course of their development.

This specification is a revised version of the previous version 1.0. The following factors were taken into consideration in the production of this revised edition.

- Although Version 1.0 was produced on the basis of the latest documents available relating to ISO/IEC 14443 as of March 2000, since that time, work at ISO have progressed, and with some exceptions, were released in the form of ISO standards. It was therefore necessary to achieve compatibility with these ISO standards.
- Following the release of Version 1.0, requests were made from various fields asking for implementation specifications for PCD (open PCD) that will enable the operation of placing or holding up a card. Implementation specifications were therefore added or reviewed in order to respond to these needs.

We hope that this specification will assist in the future proliferation of IC cards and IC card systems.

Furthermore, be aware of the following when referring to or using these specifications.

- The functions, testing methods and so forth specified in these specifications are subject to addition, revision, alteration or deletion during the course of substantive testing and other efforts scheduled to be conducted in the future by this association.
- This association is not responsible in any way for the contents of these specifications or the results of their use, including industrial property rights and so forth.

In conclusion, the association would like to express its deep appreciation to the RW compatibility verification work group (located within the New Media Development Association) for its numerous contributions and constructive discussions, and to those persons at the Ministry of Economics, Trade and Industry for their generous support of those efforts pertaining to the production of these specifications.

July 2001

New Media Development Association

## Table of contents

1.	SYSTEM OVERVIEW .....	1
2.	DESIGN GUIDELINES.....	2
2.1	INTRODUCTION .....	2
2.2	CHARACTERISTICS OF ASSUMED PICC AND PCD .....	3
2.3	CHARACTERISTICS OF THIS IMPLEMENTATION SPECIFICATION .....	5
2.4	DOMESTIC RADIO LAW .....	7
2.5	CITED STANDARDS .....	8
2.6	OTHERS .....	9
3.	COMPONENTS .....	10
4.	USAGE CONDITIONS .....	13
4.1	BASIC GUIDELINES .....	13
4.2	BASIC CONDITIONS .....	14
5.	CARD ANTENNA CHARACTERISTICS .....	16
5.1	ANTENNA SHAPE.....	16
5.2	ANTENNA RESISTANCE VALUE.....	17
5.3	INDUCTANCE .....	18
5.4	RESONANCE FREQUENCY .....	19
5.5	MATERIAL AND PRODUCTION METHOD .....	20
6.	CARD IC CHARACTERISTICS.....	21
6.1	OPERATING POWER.....	21
6.2	INPUT SIGNAL .....	24
6.3	OUTPUT SIGNAL.....	25
7.	PCD ANTENNA CHARACTERISTICS.....	26
7.1	ANTENNA POSITION .....	26
7.2	ANTENNA SHAPE.....	27
7.3	ANTENNA RESISTANCE VALUE.....	28
7.4	INDUCTANCE .....	29
7.5	RESONANCE FREQUENCY .....	30
7.6	MATERIAL AND PRODUCTION METHOD .....	31
8.	POWER TRANSMISSION .....	32
8.1	FREQUENCY .....	32
8.2	OPERATING MAGNETIC FIELD .....	33
8.2.1	PICC Operating Magnetic Field .....	33
8.2.2	PCD Generated Magnetic Field.....	34
9.	COMMUNICATION PCD TO PICC .....	35
9.1	COMMUNICATION SIGNAL INTERFACE TYPE A .....	35
9.1.1	Bit Rate .....	35
9.1.2	Modulation .....	36
9.1.3	Bit Representation and Coding.....	39

9.2	COMMUNICATION SIGNAL INTERFACE TYPE B .....	40
9.2.1	Bit Rate .....	40
9.2.2	Modulation.....	41
9.2.3	Bit Representation and Coding.....	42
10.	COMMUNICATION PICC TO PCD .....	43
10.1	COMMUNICATION SIGNAL INTERFACE TYPE A .....	43
10.1.1	Bit Rate .....	43
10.1.2	Load Modulation.....	44
10.1.3	Subcarrier .....	45
10.1.4	Subcarrier Modulation Method.....	46
10.1.5	Bit Representation and Coding.....	47
10.2	COMMUNICATION SIGNAL INTERFACE TYPE B .....	48
10.2.1	Bit Rate .....	48
10.2.2	Load Modulation.....	49
10.2.3	Subcarrier .....	50
10.2.4	Subcarrier Modulation .....	51
10.2.5	Bit Representation and Coding.....	52
11.	POLLING .....	53
12.	ANTICOLLISION .....	55
12.1	TYPE A-INITIALIZATION AND ANTICOLLISION.....	59
12.1.1	Frame Format and Timing.....	59
12.1.2	PICC States.....	70
12.1.3	Command Set.....	80
12.1.4	Select Sequence .....	84
12.2	TYPE B - INITIALIZATION AND ANTICOLLISION.....	99
12.2.1	Character, Frame Format and Timing .....	99
12.2.2	Cyclic Redundancy Check Code (CRC_B) .....	107
12.2.3	Anticollision Sequence.....	108
12.2.4	PICC States Description .....	109
12.2.5	Command Set.....	119
12.2.6	Anticollision Response Rules .....	120
12.2.7	REQB/WUPB Command .....	122
12.2.8	Slot Marker Command (Slot_MARKER).....	129
12.2.9	Answer to Request (ATQB) .....	132
12.2.10	ATTRIB Command.....	140
12.2.11	Answer to ATTRIB Command.....	149
12.2.12	HLTB Command and Answer.....	151
12.3	COMMUNICATION EXAMPLE TYPE A.....	152
12.3.1	Overview of Communication Example of Bit Frame Anticollision Processing .....	152
12.3.2	Explanation of Selection Processing of Bit Frame Anticollision.....	155
12.4	CRC_A AND CRC_B ENCODING .....	158
12.4.1	CRC_A Encoding.....	158
12.4.2	CRC_B Encoding .....	161
12.4.3	Code Sample Written in C Language for CRC Calculation.....	165

12.5	TYPE A TIMESLOT - INITIALIZATION AND ANTICOLLISION .....	168
12.5.1	Bit, Byte and Frame Format.....	169
12.5.2	PICC States.....	171
12.5.3	Command/Response Sets .....	176
12.5.4	Time Slot Type Anticollision Processing.....	179
12.6	EXAMPLE OF ANTICOLLISION SEQUENCE FOR TYPE B.....	182
13.	TRANSMISSION PROTOCOL .....	187
13.1	PROTOCOL ACTIVATION OF PICC TYPE A .....	190
13.1.1	Request for Answer to Select .....	193
13.1.2	Answer to Select (ATS).....	195
13.1.3	Protocol and Parameter Selection Request .....	203
13.1.4	Protocol and Parameter Selection Response.....	207
13.1.5	Activation Frame Waiting Time .....	208
13.1.6	Error Detection and Recovery.....	209
13.2	PROTOCOL ACTIVATION OF PICC TYPE B.....	212
13.3	HALF-DUPLEX BLOCK TRANSMISSION PROTOCOL.....	213
13.3.1	Block Format .....	214
13.3.2	Frame Waiting Time (FWT).....	221
13.3.3	Power Level Indication.....	224
13.3.4	Protocol Operation.....	225
13.4	PROTOCOL DEACTIVATION OF PICC TYPE A AND TYPE B .....	233
13.4.1	Deactivation Frame Waiting Time .....	234
13.4.2	Error Detection and Recovery.....	235
13.5	MULTI-ACTIVATION EXAMPLE .....	236
13.6	PROTOCOL SCENARIOS.....	237
13.6.1	Error-free Operation.....	239
13.6.2	Error handling .....	243
13.7	BLOCK AND FRAME CODING OVERVIEW .....	252
13.8	T=1 PROTOCOL USAGE SPECIFICATIONS.....	254
13.8.1	PICC Activation .....	255
13.8.2	Protocol Processing.....	257
13.9	TRANSMISSION CONTROL MATRIX OF T=CL PROTOCOL (REFERENCE) .....	263
14.	CARD TEST METHODS .....	267
14.1	TEST ENVIRONMENT.....	267
14.2	TEST APPARATUS.....	268
14.2.1	Calibration Coil .....	269
14.2.2	Test PCD .....	273
14.2.3	Test PCD-S.....	285
14.2.4	Digital Sampling Oscilloscope.....	289
14.3	TEST METHODS.....	290
14.3.1	Testing Using Test PCD .....	290
14.3.2	Testing Using Test PCD-S.....	298
15.	PCD TEST METHODS.....	299

15.1	TEST ENVIRONMENT.....	299
15.2	TEST APPARATUS.....	300
15.2.1	Reference PICC.....	301
15.3	TEST METHODS.....	312
15.3.1	Magnetic Field Strength .....	312
15.3.2	Power Transmission Test .....	316
15.3.3	Modulation Waveform .....	318
15.3.4	Reception Ability of Load Modulation Signal.....	320
16.	EXTERNAL COMMUNICATION PROTOCOL.....	322
16.1	PHYSICAL INTERFACE .....	322
16.2	BLOCK FORMAT.....	324
16.2.1	RCB (Required).....	325
16.2.2	LEN (Required).....	326
16.2.3	DAT (Optional).....	327
16.2.4	BCC (Required).....	328
16.3	COMMUNICATION TIME SPECIFICATIONS .....	329
16.3.1	Character Waiting Time (CWT) .....	330
16.3.2	Block Guard Time (BGT).....	331
16.3.3	Block Waiting Time (BWT) .....	332
16.4	COMMUNICATION ERROR PROCESSING .....	333
16.4.1	PCD Communication Error Processing .....	333
16.4.2	Upper Device Communication Error Processing .....	335
16.5	COMMANDS AND RESPONSES.....	337
16.5.1	Commands and Response for PICC .....	337
16.5.2	Summary of Commands and Responses for PCD .....	340
16.5.3	Details of Commands and Responses for PCD.....	344
16.6	REFERENCE INFORMATION .....	377
16.6.1	Normal Communication Sequence Examples .....	377
16.6.2	Abnormal Communication Sequence Example.....	382
17.	COMPATIBILITY TEST METHOD .....	388
[REFERENCE]	EXAMPLE OF COMPATIBILITY VERIFICATION SHEET .....	390

## 1. System Overview

These proximity communication interface implementation specification define specifications and standards that supplement ISO/IEC 14443-2, 3 and 4 with respect to functions pertaining to contactless communication between the PICC and PCD. Therefore, these specifications attempt to ensure interoperability and compatibility of various types of PICCs and PCDs of numerous manufacturers by serving to standardize antenna characteristics, resonance characteristics and various other parameters at the production level not defined by ISO.

These implementation specifications apply to PICC based on the radio wave interface type of ASK 100% modulation type A or ASK 10% modulation type B as indicated in ISO/IEC 14443-2 as well as PCD capable of operating both of these cards.

The range over which this implementation specification are applicable is shown in "Fig. 1-1 Target of Proximity Communication Interface Implementation Specifications".

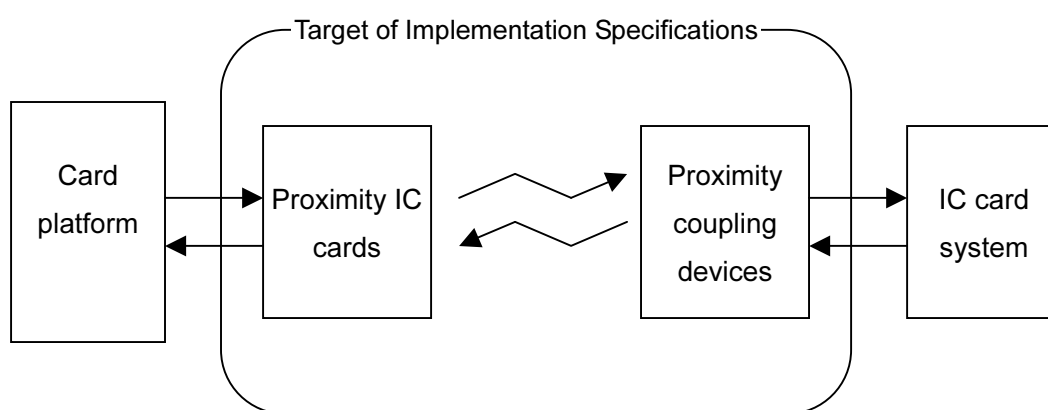


Fig. 1-1 Target of Proximity Communication Interface Implementation Specifications

## 2. Design Guidelines

### 2.1 Introduction

Proximity communication interface implementation standards are produced to ensure interoperability and compatibility between PICC and PCD under specific usage conditions indicated in "4. Usage Conditions". These are discussed in ISO/IEC specifications (ISO/IEC 14443 PICC Specifications) so as not to inhibit the extendability and diversity of usage conditions. Accordingly, it is necessary to add to and alter ISO/IEC specifications in order to ensure compatibility based on the premise of certain specific usage conditions.

To begin with, in this implementation specification, ISO/IEC specifications are defined and described as "Basic Specifications" in the sense of serving as the basis of this implementation specification.

Next, specifications that are added in the form of implementation specifications are defined and described as "Extended Specifications" in the sense of being an extension to the basic specifications.

Moreover, those specifications not included in "basic specifications" or "extended specifications" for which implementation is preferable but not required are defined and described as "References".



## 2.2 Characteristics of Assumed PICC and PCD

The IC card systems assumed in these implementation specifications are characterized by enhanced security functions for which there are new needs with respect to PICC. Consequently, it is necessary to consider the matters indicated below.

### (1) PICC Equipped with an Encryption Coprocessor

When implementing encryption processing such as public key encryption (ex. RSA) within an IC card, the current technology calls for an independent encryption coprocessor within the card IC for processing. This IC requires power consumption of roughly 50 mW or more. In this case, it is estimated that at least 100 mW will be required for the output of the PCD.

While a communication distance of about 10 cm is said to be required in the case of ticket gates of transportation means, it is not easy to achieve this communication distance with a PICC having power consumption of 50 mW or more. However, since there is a considerable likelihood that IC power consumption will be reduced and revisions will be made to domestic the Radio related law in the future, there is a possibility that communication distance will increase. Thus, it is necessary to specify the antenna size of the PICC with the potential for future development in mind. In order to achieve longer communication distances, it will be desirable to specify antenna sizes to be as large as possible.

### (2) Single Card Operation and Two Card Operation

In the case of PICC, there are two possible operating forms: namely, an operating form in which only a single PICC communicates with a single PCD in the same manner as conventional contact IC cards (single card operation), and an operating form in which multiple PICCs establish links with a single PCD to communicate with that device (multiple card operation). Specifically, when the number of cards in multiple card operation is limited to two cards, it is referred to as a two card operation.

Single card operation is used in systems premised on processing with a single specific card. Two card operation is used in systems in which a PCD simultaneously establishes a link with two PICCs and uses each card for different roles, such as using the first PICC for a specific application, and the second PICC for payment for instance.

Caution is required in that, depending on which of these operation forms is assumed, the resonance frequency of the PICC and other design conditions vary. Although a PICC inherently premised on two card operation can also be used for single card operation enabling it to cover both forms of operation, since a system with the longest communication distance as possible may be implemented on the premise of single card operation, this implementation specification allows both PICC premised on single card operation and PICC premised on two card operation.

### (3) Open PCD

In the case of contactless applications, received power basically decreases the farther away from the antenna. If an encryption coprocessors requiring large power consumption is loaded, with the present level of technology, it is necessary to bring the card close to the PCD. In such cases as well, from the viewpoint of ease of operation and ease of maintenance of the PCD, there is a desire to simply place or hold the card near the PCD without actually inserting the card into the slot of the PCD. A system mounted with an open PCD is preferable for such needs.

It is necessary for the PCD to comply with the existing domestic Radio laws for each of its antenna outputs (see "2.4 Domestic Radio Law"). Assuming the power consumption of a card IC to be about 50 mW, the PCD is assumed to be a premises radio station or convenience radio station.

If reductions in power consumption of card ICs progress and the output of PCD falls below 50 mW in the future, it may be possible to realize PCD that function as radio stations that do not require a license as with extremely low power radio stations.

### (4) Slot-In Type PCD

Even with PICCs, in cases in which card processing requires a relatively long period of time at government offices and financial institutions, for example, in order to perform processing reliably, there have been requests from users indicating the desire to perform card processing with the card slipped into the PCD. In such cases, a system implemented with a slot-in type of PCD will be required.

When considering the convenience of performing official clerical procedures by users, it is desirable to suppress the antenna output to the range of extremely low power radio and use as an extremely low power radio station. However, with the slot-in type PCD, while supplying the required power to the card inside the PCD, the entire PCD is shielded thereby avoiding radiation outside the PCD and making it possible to suppress the output of radio waves to the outside for the entire PCD to within the range of an extremely low power radio station.

## 2.3 Characteristics of This Implementation Specification

The matters indicated below have been taken into consideration in this implementation specification.

### (1) Improvement of Compatibility of between PICCs and PCDs

This implementation specification were produced for the purpose of improving compatibility between PICC and PCD as indicated in "2.2 Characteristics of Assumed PICC and PCD". However, considerations have also been given to allow a certain degree of freedom in the design of PICC and PCD. It should therefore be noted that this implementation specification does not unequivocally guarantee the compatibility of PICC and PCD. In order to guarantee compatibility, users of this implementation specification expected to perform the PICC and PCD test methods indicated in Chapters 14 and 15, along with the operation tests for PICC and PCD actually used in the IC card system to be applied.

### (2) Need for Specifications other than ISO/IEC Standards

ISO/IEC standards specify specifications oriented toward maintaining higher levels of extendability (or diversity). In addition, discussions are presented focusing mainly on remote functions. Consequently, the operating specifications of a PICC are specified as, for example, "Shall operate as intended in a magnetic field from 1.5 A/m to 7.5 A/m". The antenna diameter of the test PCD is 15 cm and also is premised to a certain extent on remote functions. In addition, the fact that specifications are basically based on magnetic field strength suggests that these standards are premised on that the PICC and PCD being arranged at a distance at which they do not exert mutual effects, and that a uniform magnetic field be formed.

In contrast, since this project assumes power consumption of the card IC to be around 50 mW, the PICC and PCD are arranged in a relationship such that they are in close physical proximity and that they mutually affect the physical and electrical characteristics of the antenna. It is extremely unlikely that the measuring instrument with a uniform magnetic field is identical to the actual magnetic field detected by the PICC. This point is not specified in ISO/IEC standards, and is the most characteristic point of this implementation specification.

### (3) Required Specifications other than ISO/IEC Standards

It is necessary to add the matters indicated below not described in ISO/IEC standards for the reasons described in the previous section. In other words, these are the important points of this implementation specification.

- (a) PICC specifications (antenna shape, etc.)  
See "5. Card Antenna Characteristics".
- (b) Reference (surface reading type) PCD specifications for evaluation of PICC  
See "14. Card Test Methods".
- (c) PCD specifications (antenna shape, etc.)  
See "7. PCD Antenna Characteristics".
- (d) Reference PICC specifications for evaluation of PCD  
See "15. PCD Test Methods".
- (e) Protocol between external devices and PCD (reference specifications)  
See "16. External Communication Protocol".

## 2.4 Domestic Radio Law

For reference purposes, the relationship between radio stations and power consumption for a frequency of 13.56 MHz in Japan is shown in "Table 2.4-1 References: Domestic Radio Stations (13.56 MHz  $\pm$  7 KHz) Rules and Power Consumption".

Table 2.4-1 References: Domestic Radio Stations (13.56 MHz  $\pm$  7 KHz) Rules and Power Consumption

Power consumption	Rule	Extremely low power radio stations	Premise radio stations or convenience radio stations	Specified low power
		54 dBmV/m or less (at 3 m) (Antenna output about 50 mW or less <sup>*1</sup> )	Antenna output 1 W or less (equal to extremely low power radio stations outside the 13.56 MHz $\pm$ 7 KHz band)	Antenna output 10 mW
		Radio license not required	Technical competence required, radio station application required	Technical competence required, radio station license not required
Current example: No CPU Power consumption: 2-5 mW		About several cm	About 10 cm	About 5 mm
PICC Power consumption: 10-20 mW		About 5 mm (surface reading)	About several cm	Not possible
New generation IC card CPU + encryption coprocessor Power consumption: 25 mW or more		About 5 mm (surface reading) shielded	-	Not possible

\*1: Reference value assuming an antenna diameter of 30 mm

## 2.5 Cited Standards

The standards cited in these implementation specifications are indicated in "Table 2.5-1 Cited Standards".

Table 2.5-1 Cited Standards

Standard number	Title	Publication
ISO/IEC 14443-1	Identification cards-Contactless integrated circuit (s) cards - Proximity cards - Part1 : Physical characteristics	First edition 2000-04-15
ISO/IEC 14443-2	Identification cards-Contactless integrated circuit (s) cards - Proximity cards - Part2 : Radio frequency power and signal interface	FDIS 2000-05-02
ISO/IEC 14443-3	Identification cards-Contactless integrated circuit (s) cards - Proximity cards Part3 : Initialization and anticollision	First edition 2001-02-01
ISO/IEC 14443-4	Identification cards-Contactless integrated circuit (s) cards - Proximity cards Part4 : Transmission protocol	First edition 2001-02-01
ISO/IEC 10373-6	Identification cards - Test methods - Part4 : Proximity cards	FDIS 2001-01-18
ISO/IEC 7810	Identification cards - Physical characteristics	2nd edition 1995-08-15
ISO/IEC 7816-2	Identification cards - Integrated circuit(s) cards with contacts - Part2 : Dimensions and location of the contacts	First edition 1999-03-01

## 2.6 Others

Dimensions and values not having tolerances described in this implementation specification are treated as reference dimensions or reference values, and refer to the target central dimension and central value.

### 3. Components

This Proximity Communication Interface Implementation Specification stipulate specifications and standards that supplement ISO/IEC 14443-2, 3 and 4 with respect to functions relating to contactless communications in PICC and external nodes.

This implementation specification applies to PICC based on the radio wave interface type of ASK 100% modulation type A or ASK 10% modulation type B indicated in ISO/IEC 14443-2, as well as PCD capable of operating both of these cards.

The components of this proximity communication interface implementation specification is indicated in "Fig. 3-1 Components of the Proximity Communication Interface Implementation Specification".

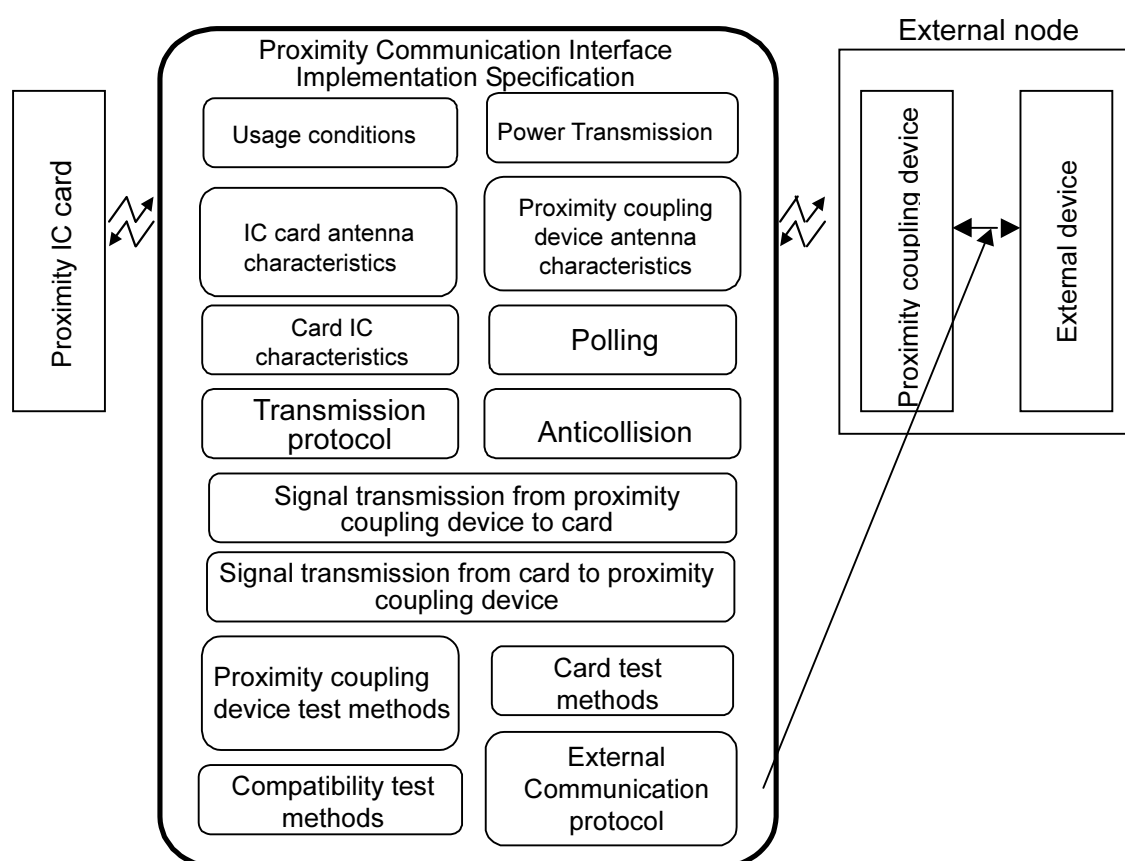


Fig. 3-1 Components of the Proximity Communication Interface Implementation Specification

The sub-categories in the main category of "Proximity Communication Interface Implementation Specification" are specified in "Table 3-1 Functional Components".



Table 3-1 Functional Components

Chapter Title	Description
Usage Conditions	Specifies the usage conditions of the proximity communication interface assumed in applications. The specified usage conditions include communication range, number of cards used, type of card used and applicable radio law.
Card Antenna Characteristics	Antenna shape, antenna resistance value and other characteristics are specified as PICC antenna characteristics. Antenna characteristics are to be specified with difference in characteristics due to antenna material and production method in mind.
Card IC Characteristics	Characteristic values including IC power consumption and operating voltage are specified as IC characteristics for PICC. IC characteristics are to be specified with difference in characteristics due to IC function and production method in mind.
PCD Antenna Characteristics	Antenna position, shape and other characteristics are specified as PCD antenna characteristics. Antenna characteristics are to be specified with differences in characteristics due to communication performance and production method in mind.
Power Transmission	In addition to specifying power transmission characteristics of the PCD based on ISO/IEC 14443-2, power transmission characteristics of the PCD are specified in consideration of the PCD characteristics and card characteristics as specified in these implementation specifications.
Signal Transmission from PCD to Card	The modulation method, modulation waveform and encoding method of signal transmission from the PCD to the PICC are specified on the basis of ISO/IEC 14443-2. Type A and Type B communication methods are specified.
Signal Transmission from Card to PCD	The modulation method and encoding method of signal transmission from the PICC to the PCD are specified on the basis of ISO/IEC 14443-2. Type A and Type B communication methods are specified.
Polling	Polling is specified based on ISO/IEC 14443-3 as a method for detecting whether or not a PICC capable of communicating with the PCD is present. Polling methods are specified that are compatible with both type A and type B communication methods.

Table 3-1 Functional Components (continued)

Chapter Title	Description
Anticollision	Anticollision avoidance is specified on the basis of ISO/IEC 14443-3 for acquiring identification information of PICC even when multiple PICCs capable of communicating with the PCD are present. Communication methods are specified for both type A and type B. The method for type A is to be the time slot method.
Transmission Protocol	Communication frames and the basic communication sequence are specified with the transmission protocol of the PICC and PCD on the basis of ISO/IEC 14443-4. Type A and Type B communication formats are specified.
Card Test Methods	Specifies the PICC test methods specified with ISO/IEC 10373-6, while also specifying the test method of PICC in consideration of the characteristics and so forth of the PCD as specified in this implementation specification for the purpose of evaluating PICC.
PCD Test Methods	In addition to specifying test methods of the PCD based on ISO/IEC 10373-6, test methods of the PCD are specified in consideration of PICC characteristics specified in this implementation specification for the purpose of evaluating the PCD.
External Communication Protocol	Commands and responses required for realizing a proximity communication interface in the communication protocol between the PCD and an external device are specified. Type A and type B communication formats are specified. The method for type A is to be the time slot method.
Compatibility Test Methods	The test method is specified for evaluating interoperability and compatibility of a PICC and PCD. The contents of evaluation by cross-testing the PICC and PCD are also specified.

## 4. Usage Conditions

The following specifies the usage conditions of the proximity communication interface assumed in this implementation specification. The specified usage conditions include communication range, number of cards used, type of card used and applicable radio telegraphy law.

### 4.1 Basic Guidelines

Basic guidelines for drafting the usage conditions are indicated below.

- (1) Basic conditions are assumed with the focus on ensuring the safety of personal authorization such as issuing/confirmation of certificates and reserving/using public facilities as examples of applications in public fields.
- (2) PICC are assumed to be proximity contactless type cards that comply with ISO/IEC 14443 and which have a built-in chip containing a CPU and encryption coprocessor.
- (3) The electromagnetic waves generated from the PCD are assumed to be within the range of extremely low power radio waves in the case of slot-in PCD. In the case of open PCD, considering the current level of technology, the electromagnetic waves generated from the PCD are assumed to constitute an output that exceeds extremely low power radio waves.

## 4.2 Basic Conditions

Basic conditions relating to usage conditions are indicated in "Table 4.2-1 Basic Conditions".

Table 4.2-1 Basic Conditions

No.	Item	Description
1	Usage form	<p>The following two usage forms are assumed.</p> <p>(1) Card is placed or held over the PCD (in the case of an open PCD).</p> <p>(2) Card is inserted into a slot or box equipped on the PCD (in the case of a slot-in PCD).</p> <p>In either case, the direction of card insertion or orientation of the card is not significant.</p>
2	Type of PICC	<p>The following two types are assumed.</p> <p>(1) Type A specified in ISO/IEC 14443-2</p> <p>(2) Type B specified in ISO/IEC 14443-2</p>
3	No. of cards operated	<p>Only one card is assumed in the case of PICC premised on single card operation. One to two cards are assumed in the case of PICC premised on two card operation. However, the operated PICCs working in combination are assumed to be of the same type (type A cards or type B cards), and operation of combinations of different types of cards is not specified in this implementation specification.</p>
4	Applicable radio law	<p>Shall be based on the Radio Law applied in Japan.</p>

Table 4.2-1 Basic Conditions (continued)

No.	Item	Description
5	Communication range	<p>A distance of 0-5 mm (*1) and dislocation diameter of about 5 mm (*2) are assumed in the case of slot-in PCD, while a distance of 0-20 mm and dislocation diameter of about 20 mm are assumed in the case of open PCD. However, this does not exclude communication outside this range. Furthermore, if held within holders (or other containers that hold the card), the range shall be within such holder.</p> <p>*1: Distance refers to the distance to the surface opposing the PCD side of the PICC assuming the surface of the PCD casing to be 0 mm (origin) and the antenna of the PICC and the PCD are held horizontally.</p> <p>*2 Dislocation refers to the amount of dislocation in the horizontal direction of the PICC assuming the reading center of the PCD and center of the outer diameter of the PICC are aligned to be 0 mm (origin) and the antenna of the PICC and the PCD are held horizontally.</p>
6	PICC physical specifications	Shall be ID-1 specified in ISO/IEC 14443-1. However, thickness less than or equal to ID-1 are also allowed.

## 5. Card Antenna Characteristics

Antenna shape, antenna resistance value and other characteristics are specified as PICC antenna characteristics. Antenna characteristics shall be specified with consideration to differences in characteristics due to antenna material and production methods.

### 5.1 Antenna Shape

#### (1) Basic Specifications

Although there are basically no particular restrictions on the shape and position of the antenna allocation in PICC, the position indicated in "Fig. 5.1-1 Minimum Coupling Area of PICC" shall be included.

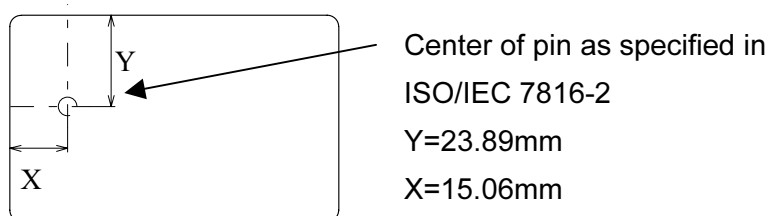


Fig. 5.1-1 Minimum Coupling Area of PICC

#### (2) Extended Specifications

In order to operate the PICC in four direction (front, back, up, down), the antenna mounting area shall be where the coupling area will be minimum with respect to all directions. The antenna allocation range is shown with diagonal lines in "Fig. 5.1-2 Antenna Mounting Range".

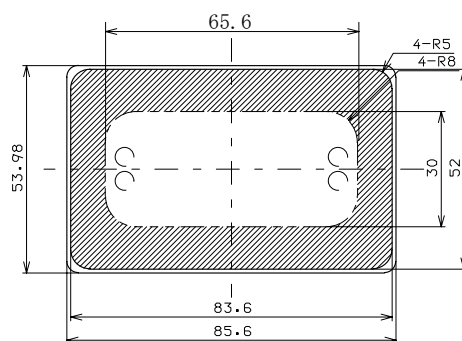


Fig. 5.1-2 Antenna Mounting Range

#### (3) References

None

## 5.2 Antenna Resistance Value

### (1) Basic Specifications

None

### (2) Extended Specifications

Although resistance values are not particularly specified in this specification, the resistance value shall at least satisfy the specifications specified in the following:

"8. Power Transmission"

"9. Communication PCD to PICC"

"10. Communication PICC to PCD"

"14. Card Test Methods"

### (3) References

None

### 5.3 Inductance

#### (1) Basic Specifications

None

#### (2) Extended Specifications

Although inductance are not particularly specified in this specification, the inductance value shall at least satisfy the specifications specified in the following:

"8. Power Transmission"

"9. Communication PCD to PICC"

"10. Communication PICC to PCD"

"14. Card Test Methods"

#### (3) References

None



## 5.4 Resonance Frequency

### (1) Basic Specifications

None

### (2) Extended Specifications

The resonance frequencies when using a single PICC and when superimposing two cards are specified.

#### (a) When Using a Single Card

The resonance frequency is preferably 19 MHz or higher, and shall at least satisfy the specifications specified in the following:

"8. Power Transfer"

"9. Communication PCD to PICC"

"10. Communication PICC to PCD"

"14. Card Test Methods"

Furthermore, in the case of card premised on single card operation, the resonance frequency may be 19 MHz or lower, but considerations must be given to the effects when bringing the card in close proximity of a PCD.

In addition, in the case of using superimposed cards, a resonance frequency that satisfies the specification in "5.4 (2) (b) When Superimposing Two Cards" shall be selected.

Resonance frequency shall be measured using the method specified in the "NOTE" of section "15.3.1 (1) (a) a) 2)".

#### (b) When Superimposing Two Cards

The resonance frequency is preferably 13 MHz or higher, and shall at least satisfy the specifications specified in the following:

"8. Power Transmission"

"9. Communication PCD to PICC"

"10. Communication PICC to PCD"

"14. Card Test Methods"

Resonance frequency shall be measured using the method specified in the "NOTE" of section "15.3.1 (1) (a) a) 2)".

### (3) References

None

## 5.5 Material and Production Method

### (1) Basic Specifications

None

### (2) Extended Specifications

Although materials and production methods are not particularly specified in this specification, materials and production methods shall at least satisfy the specifications specified in the following:

"8. Power Transmission"

"9. Communication PCD to PICC"

"10. Communication PICC to PCD"

"14. Card Test Methods"

### (3) References

None

## 6. Card IC Characteristics

Characteristic values including IC power consumption and operating voltage are specified as IC characteristics for PICC. IC characteristics shall be specified with consideration to differences in characteristics due to IC function and production methods.

### 6.1 Operating Power

#### (1) Basic Specifications

None

#### (2) Extended Specifications

The power supply method, minimum operating power, maximum operating power, maximum input power and input capacity of card ICs are specified.

##### (a) Power Supply Method

The card IC shall operate by receiving power supplied from the PCD through an antenna.

##### (b) Minimum Operating Power

There are no particular specifications for the value of minimum power consumption at which the card IC functions normally. However, the power shall be appropriate for the card IC to operate at the minimum operating magnetic field specified in "14. Card Test Methods".

Section "6.1 (2) (e) Definition of Power Consumption" is applied for the power consumption of the card IC.

##### (c) Maximum Operating Power

There are no particular specifications for the maximum power consumption at which the card IC functions normally. However, the power shall be appropriate for the card IC to operate at the maximum operating magnetic field specified in "14. Card Test Methods".

Section "6.1 (2) (e) Definition of Power Consumption" is applied for the power consumption of the card IC.

##### (d) Maximum Input Power

There are no particular specifications for the value of maximum input power at which the card IC is not destroyed. However, the power shall be that at which the card IC is not destroyed at the maximum applied magnetic field specified in "14. Card Test Methods".

## (e) Definition of Power Consumption

The card IC equivalent circuit and its components are shown in "Fig. 6.1-1 Card IC Equivalent Circuit 1" and "Table 6.1-1 Equivalent Circuit Composition". Card IC power consumption shall be the power that is consumed by load resistor R1 in order to correspond to the Reference PICC circuit drawing specified in Annex D of ISO/IEC 10373-6.

If the rectifier characteristics differ between the card IC and card IC equivalent circuit 1, the power shall be that resulting from converting the card IC rectifier characteristics to the rectifier characteristics of card IC equivalent circuit 1.

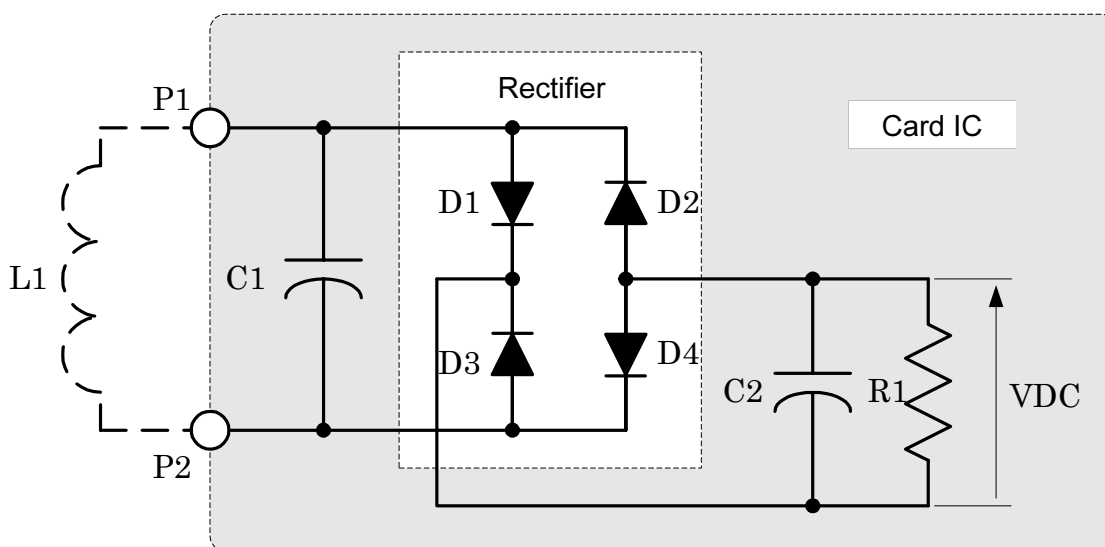


Fig. 6.1-1 Card IC Equivalent Circuit 1

Table 6.1-1 Equivalent Circuit Composition

Symbol	Components	Part constant and type
P1, P2	Coil connection pad	-
C1	Input capacity	As per "(f) Input Capacity"
D1, D2, D3, D4	Full wave rectifier diode	Schottky diode (equivalent to BAR43)
C2	Smoothing capacitor	Determined by producing manufacturer
R1	Load resistor	Determined by producing manufacturer
VDC	Receiving voltage	Determined by producing manufacturer
L1	Antenna	-

(f) Input Capacity

There are no particular specifications for card IC input capacity. However, capacity shall satisfy "5.4 Resonance Frequency" with the antenna connected.

(3) References

None

## 6.2 Input Signal

### (1) Basic Specifications

None

### (2) Extended Specifications

The input signal that can be processed normally by the card IC is specified.

The card IC shall be able to normally process the signal specified in "9. Communication PCD to PICC" with the antenna connected. In addition, the tests specified in "14. Card Test Methods" shall be satisfied. However, the antenna connected to the card IC shall satisfy "5. Card Antenna Characteristics".

### (3) References

None

## 6.3 Output Signal

### (1) Basic Specifications

None

### (2) Extended Specifications

The output signal generated by the card IC is specified.

The card IC shall generate the signal specified in "10. Communication PICC to PCD" with the antenna connected. In addition, the tests specified in "14. Card Test Methods" shall be satisfied. However, the antenna connected to the card IC shall satisfy "5. Card Antenna Characteristics".

### (3) References

None

## 7. PCD Antenna Characteristics

Antenna position, shape and other characteristics are specified as PCD antenna characteristics. Antenna characteristics are to be specified with consideration to differences in characteristics due to communication performance and production methods.

### 7.1 Antenna Position

#### (1) Basic Specifications

None

#### (2) Extended Specifications

Although there are no particular specifications for antenna position, antenna position shall be decided so as to satisfy communication performance independent of the operating direction (front, back, up, down) of the PICC within the communication range or the coil position. In addition, the antenna shall be aligned in a direction such that the antenna of the PCD and the antenna of the PICC face each other in parallel.

An example of an antenna position of a PCD where the center of the antenna is aligned with the center of the PICC is shown in "Fig. 7.1-1 Antenna Position".

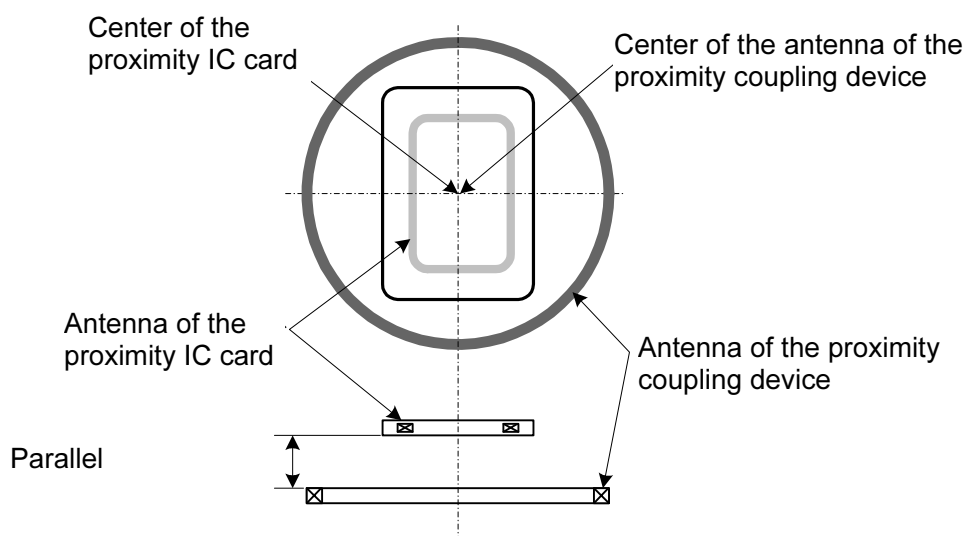


Fig. 7.1-1 Antenna Position

#### (3) References

None



## 7.2 Antenna Shape

### (1) Basic Specifications

None

### (2) Extended Specifications

The PCD antenna preferably has a symmetrical shape in order to prevent significant changes in communication performance caused by the direction of operation (front, back, up, down) of the PICC or by the coil position. An example of the antenna shape of a PCD is shown in "Fig. 7.2-1 Antenna Shape".

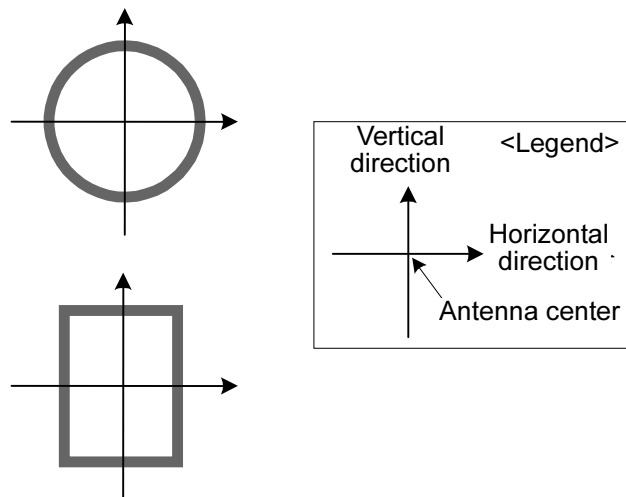


Fig. 7.2-1 Antenna Shape

### (3) References

None

### 7.3 Antenna Resistance Value

#### (1) Basic Specifications

None

#### (2) Extended Specifications

Although resistance values are not particularly specified in this specification, the resistance value shall at least satisfy the specifications specified in the following:

"8. Power Transmission"

"9. Communication PCD to PICC"

"10. Communication PICC to PCD"

"15. PCD Test Methods"

#### (3) References

None

## 7.4 Inductance

### (1) Basic Specifications

None

### (2) Extended Specifications

Although inductance are not particularly specified in this specification, inductance shall at least satisfy the specifications specified in the following:

"8. Power Transmission"

"9. Communication PCD to PICC"

"10. Communication PICC to PCD"

"15. PCD Test Methods"

### (3) References

None

## 7.5 Resonance Frequency

### (1) Basic Specifications

None

### (2) Extended Specifications

Although resonance frequency are not particularly specified in this specification, resonance frequency shall at least satisfy the specifications specified in the following:

"8. Power Transfer"

"9. Communication PCD to PICC"

"10. Communication PICC to PCD"

"15. PCD Test Methods"

### (3) References

None

## 7.6 Material and Production Method

### (1) Basic Specifications

None

### (2) Extended Specifications

Although materials and production method are not particularly specified in this specification, materials and production methods shall at least satisfy the specifications specified in the following:

"8. Power Transmission"

"9. Communication PCD to PICC"

"10. Communication PICC to PCD"

"15. PCD Test Methods"

### (3) References

None

## 8. Power Transmission

In addition to specifying power transmission characteristics of the PCD based on ISO/IEC 14443-2, power transmission characteristics of the PCD are specified with consideration to the PCD characteristics and card characteristics as specified in this implementation specification.

### 8.1 Frequency

#### (1) Basic Specifications

The frequency  $f_c$  of the RF operating field shall be 13.56 MHz $\pm$ 7kHz.

#### (2) Extended Specifications

None

#### (3) References

None

## 8.2 Operating Magnetic Field

### 8.2.1 PICC Operating Magnetic Field

#### (1) Basic Specifications

##### (a) Minimum Operating Magnetic Field ( $H_{min}$ )

The minimum unmodulated operating field shall be  $H_{min}$  and has a value of 1.5 A/m (rms).

##### (b) Maximum Operating Magnetic Field ( $H_{max}$ )

The maximum unmodulated operating field shall be  $H_{max}$  and has a value of 7.5 A/m (rms).

##### (c) Operating Conditions

A PICC shall operate as intended continually between  $H_{min}$  and  $H_{max}$ .

##### (d) Maximum Applied Magnetic Field

The PICC must operate normally even after being continuously exposed to a magnetic field strength of an average magnetic field of 10 A/m (rms) at 13.56 MHz. In addition, it must also operate normally even after being exposed for 30 seconds on average to a magnetic field strength of a maximum magnetic field of 12 A/m (rms).

#### (2) Extended Specifications

##### (a) Minimum Operating Magnetic Field ( $H_{min}$ )

The strength of the minimum operating magnetic field of the PICC is to be 4 A/m (rms) in the non-modulated state.

#### (3) References

None

## 8.2.2 PCD Generated Magnetic Field

### (1) Basic Specifications

A PCD shall generate a field of at least  $H_{min}$  and not exceeding  $H_{max}$  at manufacturer specified positions (operating volume). In addition the PCD shall be capable of powering any signal reference PICC (specified in "15. PCD Test Methods") at manufacturer specified positions (operating volume).

The PCD shall not generate a field higher than the value specified in section "8.2.1 (d) Maximum Applied Magnetic Field" in any possible PICC position.

Test methods for the PCD operating field are defined in "15. PCD Test Methods".

### (2) Extended Specifications

None

### (3) References

None



## 9. Communication PCD to PICC

The modulation method, modulation waveform and encoding method of signal transmission from the PCD to the PICC are specified on the basis of ISO/IEC 14443-2. Type A and Type B communication methods are specified.

- $f_c$ : frequency of operating field (carrier frequency).
- Manchester: method of bit coding whereby a logic level during a bit duration is represented by a sequence of two defined physical state of a communication medium. The order of the physical states within the sequence defines the logical state.
- NRZ-L (Non-Return to Zero, L for level): method of bit coding whereby a logic level during a bit duration is represented by one of two defined physical states of a communication medium.

### 9.1 Communication Signal Interface Type A

#### 9.1.1 Bit Rate

##### (1) Basic Specifications

The bit rate for the transmission during initialization and anticollision shall be  $f_c/128$  (~106 kbit/s).

##### (2) Extended Specifications

None

##### (3) References

None

## 9.1.2 Modulation

### (1) Basic Specifications

Communication from PCD to PICC for a bit rate of  $f_c/128$  shall use the modulation principle of ASK 100% of the RF operating field to create a "Pause" as shown in "Fig. 9.1-1 Pause".

The envelope of the PCD field shall decrease monotonically to less than 5% of its initial value  $H_{\text{INITIAL}}$  and remain less than 5% for more than  $t_2$ . This envelope shall comply to "Fig. 9.1-1 Pause".

If the envelope of the PCD field does not decrease monotonically, the time between a local maximum and the time of passing the same value before the local maximum shall not exceed  $0.5 \mu\text{s}$ . This shall only apply if the local maximum is greater than 5% of  $H_{\text{INITIAL}}$ .

Overshoots shall remain within 90% and 110% of  $H_{\text{INITIAL}}$ .

The PICC shall detect the "End of Pause" after the field exceeds 5% of  $H_{\text{INITIAL}}$  and before it exceeds 60% of  $H_{\text{INITIAL}}$ .

However, in systems designed to handle only one card at a time,  $t_4$  need not be respected.

The waveform of end of pause is shown in "Fig. 9.1-2 Definition of "End of Pause"".

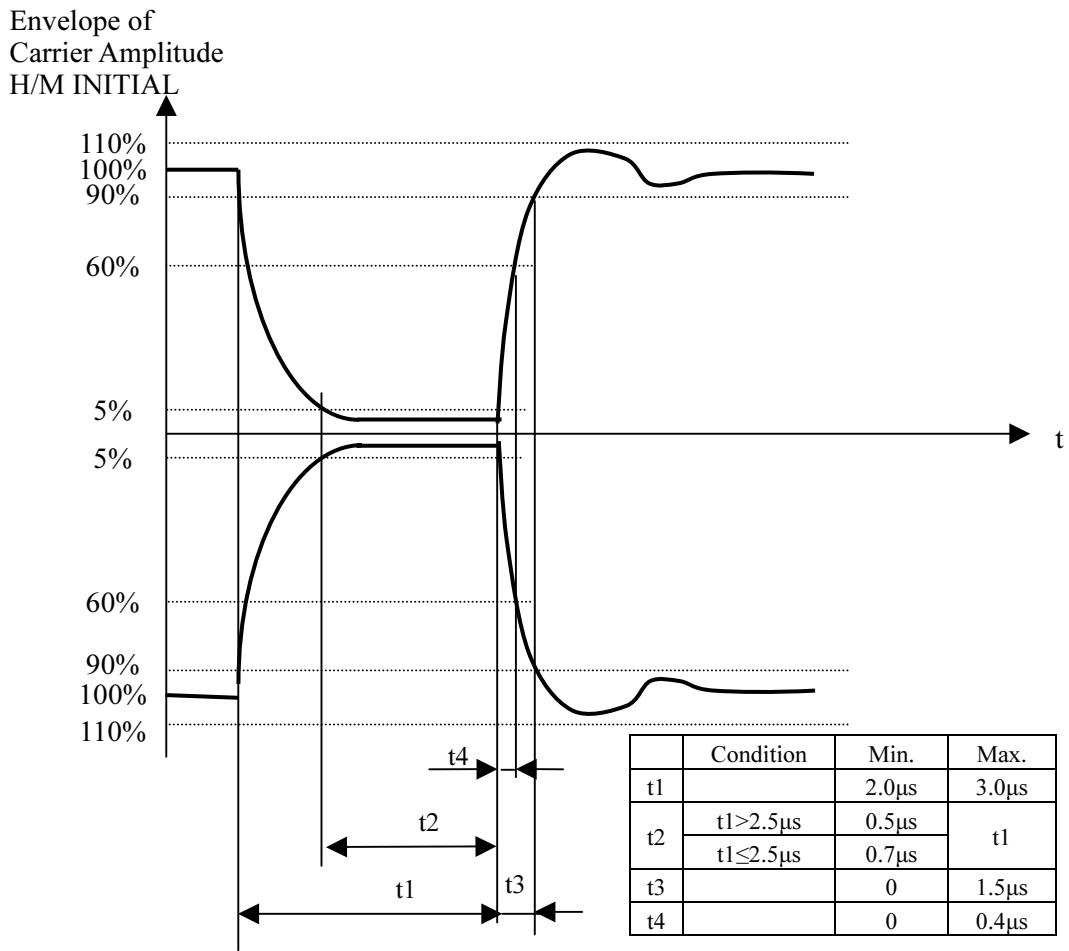


Fig. 9.1-1 Pause

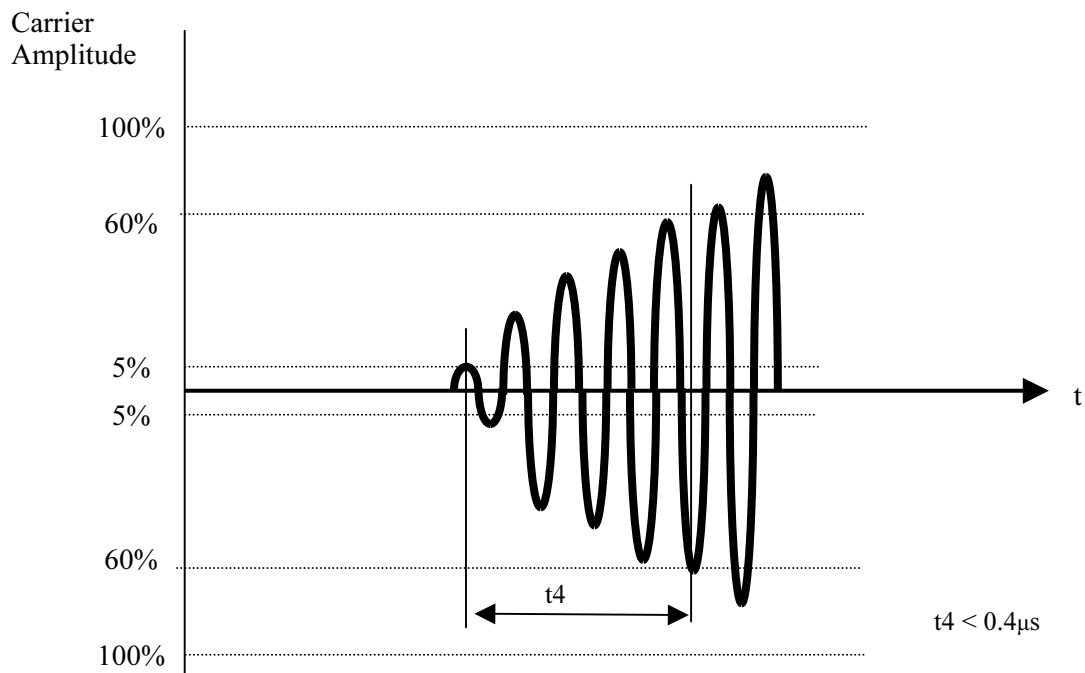


Fig. 9.1-2 Definition of "End of Pause"

## (2) Extended Specifications

None

## (3) References

None

### 9.1.3 Bit Representation and Coding

#### (1) Basic Specifications

The following sequences are defined:

- sequence X: after a time of half the bit duration a "Pause" shall occur.
- sequence Y: for the full bit duration no modulation shall occur.
- sequence Z: at the beginning of the bit duration a "Pause" shall occur.

The above sequences shall be used to code the following information:

- logic "1": sequence X
- logic "0": sequence Y with the following two exceptions:
  - If there are two or more contiguous "0"s, sequence Z shall be used from the second "0" on.
  - If the first bit after a "start of frame" is "0", sequence Z shall be used to represent this and any "0"s which follow directly thereafter.

start of communication: sequence Z

end of communication: logic "0" followed by sequence Y.

no information: at least two sequences Y.

#### (2) Extended Specifications

None

#### (3) References

None

## 9.2 Communication Signal Interface Type B

### 9.2.1 Bit Rate

#### (1) Basic Specifications

The bit rate for the transmission during initialization and anticollision shall be nominally  $f_c/128$  (~106 kbit/s). Tolerance and bit boundaries are defined in "12. Anticollision".

#### (2) Extended Specifications

None

#### (3) References

None

9.2.2 Modulation

(1) Basic Specifications

Communication from PCD to PICC shall use the modulation principle of ASK 10% of the RF operating field. The modulation index shall be between 8% and 14%. The modulation waveform shall comply to "Fig. 9.2-1 Type B Modulation Waveform". The rising and falling edges of the modulation shall be monotonic.

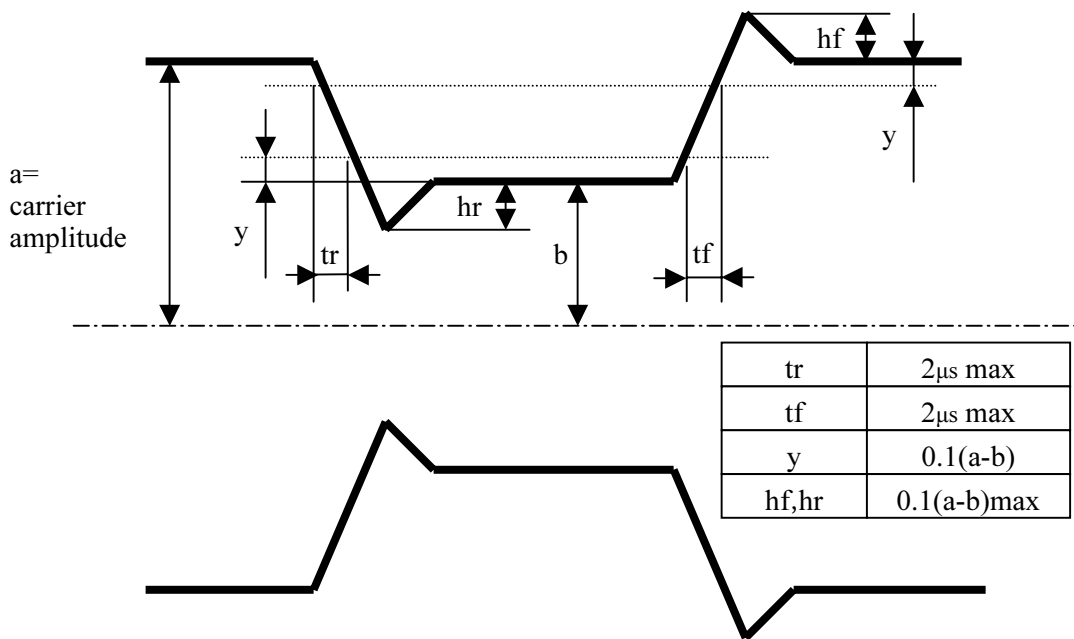


Fig. 9.2-1 Type B Modulation Waveform

(2) Extended Specifications

None

(3) References

None

### 9.2.3 Bit Representation and Coding

#### (1) Basic Specifications

Bit coding format shall be NRZ-L with logic levels defined as follows:

- Logic "1": carrier high field amplitude(no modulation applied).
- Logic "0": carrier low field amplitude.

#### (2) Extended Specifications

None

#### (3) References

None



## 10. Communication PICC to PCD

The modulation method and encoding method of signal transmission from the PICC to the PCD are specified on the basis of ISO/IEC 14443-2. Type A and Type B communication methods are specified.

The following indicates the terms and abbreviations used in this chapter.

- Subcarrier: signal of frequency  $f_s$  used to modulate a carrier of frequency  $f_c$ .
- Bit duration: time during which a logical level is defined, at the end of which a new bit starts.
- Manchester: method of bit coding whereby a logic level during a bit duration is represented by a sequence of two defined physical state of a communication medium. The order of the physical states within the sequence defines the logical state.
- BPSK (Binary Phase Shift Keying): Binary phase shift keying
- $f_s$ : Frequency of the subcarrier modulation.
- NRZ-L (Non-Return to Zero. L for level): method of bit coding whereby a logic level during a bit duration is represented by one of two defined physical states of a communication medium.

### 10.1 Communication Signal Interface Type A

#### 10.1.1 Bit Rate

##### (1) Basic Specifications

The bit rate for the transmission during initialization and anticollision shall be  $f_c/128$  (~106 kbit/s).

##### (2) Extended Specifications

None

##### (3) References

None

## 10.1.2 Load Modulation

### (1) Basic Specifications

The PICC shall be capable of communication to the PCD via a inductive coupling area where the carrier frequency is loaded to generate a subcarrier with frequency  $f_s$ . The subcarrier shall be generated by switching a load in the PICC. The load modulation amplitude shall be at least  $30/H^{1/2}$  (mV<sub>peak</sub>) when measured as described in ISO/IEC 10373-6, where H is the (rms) value of magnetic field strength in A/m.

### (2) Extended Specifications

None

### (3) References

None

### 10.1.3 Subcarrier

#### (1) Basic Specifications

The frequency  $f_s$  of the subcarrier shall be  $f_c/16$  (~847kHz). Consequently, during initialization and anticollision, one bit period is equivalent to 8 periods of the subcarrier.

#### (2) Extended Specifications

None

#### (3) References

None

#### 10.1.4 Subcarrier Modulation Method

##### (1) Basic Specifications

Every bit period shall start with a defined phase relation to the subcarrier. The bit period shall start with the loaded state of the subcarrier.

The subcarrier is modulated using On/Off keying with the sequence defined in "10.1.5 Bit Representation and Coding".

##### (2) Extended Specifications

None

##### (3) References

None

### 10.1.5 Bit Representation and Coding

#### (1) Basic Specifications

The following sequences are defined:

- sequence D: the carrier shall be modulated with the subcarrier for the first half (50%) of the bit duration.
- sequence E: the carrier shall be modulated with the subcarrier for the second half (50%) of the bit duration.
- Sequence F: the carrier is not modulated with the subcarrier for one bit duration.

Bit coding shall be Manchester with the following definitions:

- logic"1": sequence D
- logic"0": sequence E
- start of communication: sequence D
- end of communication: sequence F
- no information: no subcarrier (Sequence F)

#### (2) Extended Specifications

None

#### (3) References

None

## 10.2 Communication Signal Interface Type B

### 10.2.1 Bit Rate

#### (1) Basic Specifications

The bit rate for the transmission during initialization and anticollision shall be nominally  $f_c/128$  (~106 kbit/s).

#### (2) Extended Specifications

None

#### (3) References

None

## 10.2.2 Load Modulation

### (1) Basic Specifications

The PICC shall be capable of communication to the PCD via a inductive coupling area where the carrier frequency is loaded to generate a subcarrier with frequency  $f_s$ . The subcarrier shall be generated by switching a load in the PICC.

The load modulation amplitude shall be at least  $30/H^{1,2}$  (mV<sub>peak</sub>) when measured as described in ISO/IEC10373-6, where H is the (rms) value of magnetic field strength in A/m.

### (2) Extended Specifications

None

### (3) References

None

### 10.2.3 Subcarrier

#### (1) Basic Specifications

The frequency  $f_s$  of the subcarrier shall be  $f_c/16$  (~847kHz). Consequently, during initialization and anticollision, one bit period is equivalent to 8 periods of the subcarrier. The PICC shall generate a subcarrier only when data is to be transmitted.

#### (2) Extended Specifications

None

#### (3) References

None



## 10.2.4 Subcarrier Modulation

### (1) Basic Specifications

The subcarrier shall be BPSK modulated, see example in "Fig. 10.2-1 Allowed phase shifts" with BPSK modulation. Phase shifts shall only occur at nominal position of rising or falling edges of the subcarrier.

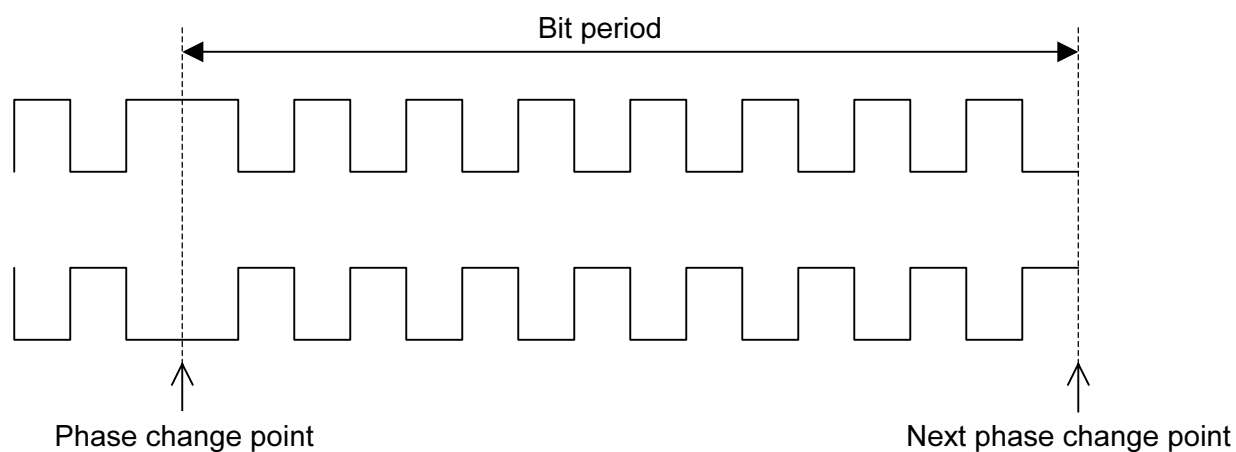


Fig. 10.2-1 Allowed Phase Shifts

### (2) Extended Specifications

None

### (3) References

None

## 10.2.5 Bit Representation and Coding

### (1) Basic Specifications

Bit coding shall be NRZ-L where a change of logic level shall be denoted by a phase shift ( $180^\circ$ ) of the subcarrier.

The initial logic level for NRZ-L at the start of a PICC frame shall be established by the following sequence:

After any command from the PCD a guard time  $TR_0$  shall apply in which the PICC shall not generate a subcarrier.  $TR_0$  shall be greater than  $64/f_s$ .

The PICC shall then generate a subcarrier with no phase transition for a synchronization time  $TR_1$ . This establishes a subcarrier phase reference  $\Phi_0$ .  $TR_1$  shall be greater than  $80/f_s$ .

This initial phase state  $\Phi_0$  of the subcarrier shall be defined as logic "1" so that the first phase transition represents a change from logic "1" to logic "0".

Subsequently the logic level is defined according to the subcarrier phase reference  $\Phi_0$ :

$\Phi_0$ : represents logic "1".

$\Phi_0 + 180^\circ$ : represents logic "0".

### (2) Extended Specifications

None

### (3) References

None

## 11. Polling

Polling for detecting existence of a PICC capable of communicating with the PCD is specified based on ISO/IEC 14443-3. Polling methods compatible with both type A and type B communication methods are specified.

The following indicates the terms and abbreviations used in this chapter.

- REQA (Request Command, Type A): Request command for a Type A PICC
- REQA (Request Command, Type B): Request command for a Type B PICC
- ATQ (Answer To Read): Response signal from PICC.

Furthermore, the PCD described in this chapter includes external devices.

## (1) Basic Specifications

In order to detect PICCs which are in the operating field, a PCD shall send repeated Request commands. The PCD shall send REQA and REQB described in "12. Anticollision" and in addition may send other commands described in "12.5 Type A Timeslot - Initialization and Anticollision".

When a PICC is exposed to an unmodulated operating field it shall be able to accept within 5ms (see "8. Power Transfer").

More specifically:

- EXAMPLE 1 When a PICC Type A receives a Type B command it shall be able to accept a REQA within 5ms of unmodulated operating field.
- EXAMPLE 2 When a PICC Type B receives any Type A command it shall be able to accept a REQB within 5ms of unmodulated operating field.

## (2) Extended Specifications

None

## (3) References

The request commands used for polling may use the encoding system described in "12.5 Type A Timeslot - Initialization and Anticollision" and REQB having an optional method. (For further details, refer to References of section "12.2.4(3)" of "12.2 Type B Initialization and Anticollision Processing".)

## 12. Anticollision

Anticollision is specified on the basis of ISO/IEC 14443-3 for acquiring identification information of PICC where multiple PICCs capable of communicating with the PCD are present. Communication methods are specified for both type A and type B.

### (1) Terms Used in this Section

- Anticollision Loop

algorithm used to prepare for dialogue between PCD and one or more PICCs out of the total number of PICCs responding to a request command

- Bit Collision Detection Protocol

Processing method which gives significance to bit units within a frame. Collision occurs when two or more PICCs send complementary bit patterns to the PCD. In the case of type A PICCs, the bit pattern overlaps and the carrier is modulated with the subcarrier for the entire bit period (100%). PCD recognizes the IDs of all PICCs in order while detecting colliding bits.

- Byte

8 bits of data designated b8 to b1, from the most significant bit (MSB, b8) to the least significant bit (LSB, b1)

- Collision

transmission by two PICCs in the same PCD energizing field and during the same time period, such that the PCD is unable to distinguish from which PICC the data originated.

- elementary time unit

etu

for "12. Anticollision", one etu is defined as  $1 \text{ etu} = 128/f_c$  (i.e.  $9.4 \mu\text{s}$  nominal)

- Frame

sequence of data bits and optional error detection bits, with frame delimiters at start and end

- Higher layer protocol

protocol layer ( not described in that makes use of the protocol layer defined in to transfer information belonging to the application or higher layers of protocol that is not described in "12. Anticollision".

- Timeslot protocol

method whereby a PCD establishes logical channels with one or more PICCs of Type B, which makes use of timeslot allocation for PICC response

- Unique Identifier

UID is the number used for anticollision processing of type A cards.

## (2) Symbols Used in this Section

- AFI	Application field identifier
	Preliminary card screening standard according to the application field.
- APa	Parameter used with ATQB
- APc	Parameter used with ATTRIB
- APf	Anticollision Prefix f, used in REQb
- APn	Anticollision Prefix n, used in Slot-MARKER Command
- ATA	Response to ATTRIB
- ATQ	Request acknowledgment signal
- ATQA	Answer To Request, Type A
- ATQB	Answer To Request, Type B
- ATTRIB	PICC selection command
- BCC	UID CLn check byte, calculated as exclusive-or over the 4 previous bytes
- CLn	Cascade Level n ( $3 \geq n \geq 1$ )
- CT	Cascade Tag (value is '88')
- CRC_A	Cyclic Redundancy Check error detection code A
- CRC_B	Cyclic Redundancy Check error detection code B
- DESEL	Deselect command
- E	End of communication, Type A
- EGT	Extra Guard Time
- EOF	End Of Frame
- etu	Elementary time unit
- FGT	Frame guard time
- fc	Carrier frequency (13.56 MHz)
- fs	Subcarrier frequency ( $fc/16$ )
- ID	IDentification number
- INF	INformation field belonging to higher layer
- LSB	Least significant bit
- MSB	Most significant bit
- N	Number of anticollision slots or PICC response probability in each slot
- n	Variable integer value as defined in the specific clause
- NAD	Node address
- NVB	Number of Valid Bits
- P	Odd Parity bit

- PARAM Attribute information parameter
- PCD Proximity coupling device for proximity IC card (including upper devices)
- PICC Proximity Card
- PUPI Pseudo-Unique PICC Identifier
- R Slot number chosen by the PICC during the anticollision sequence
- REQA Request Command, Type A
- REQB Request Command, Type B
- RFU Reserved for Future Use
- S Start of communication, Type A
- SAK Select AcKnowledge
- SEL Select code
- SOF Start of frame
- T0 Minimum time from completion of transmission by PCD to start of generation of subcarrier by PICC
- T1 Minimum time from start of generation of subcarrier to its stable generation before start of data transmission by PICC
- UID Unique identifier
- UIDn Byte number n of Unique Identifier,  $n \geq 0$

(3) For the purposes of this section, then following notation applies:

- (xxxx)b Data bit representation
- 'XX' Hexadecimal



## 12.1 Type A-Initialization and Anticollision

This section describes the initialization and collision detection protocol applicable for PICCs of Type A.

### 12.1.1 Frame Format and Timing

This section defines the frame format and timing used during communication initialization and anticollision. For bit representation and coding refer to "9. Communication PCD to PICC" and "10. Communication PICC to PCD".

#### 12.1.1.1 Frame Delay Time

##### (1) Basic Specifications

The frame delay FDT is defined as the time between two frames transmitted in opposite directions.

##### (2) Extended Specifications

None

##### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.1.1.2 Frame Delay Time PCD to PICC

#### (1) Basic Specifications

This is the time between the end of the last pause transmitted by the PCD and the first modulation edge within the start bit transmitted by the PICC and shall respect the timing defined in "Fig. 12.1-1 Frame Delay Time PCD to PICC", where  $n$  is an integer value.

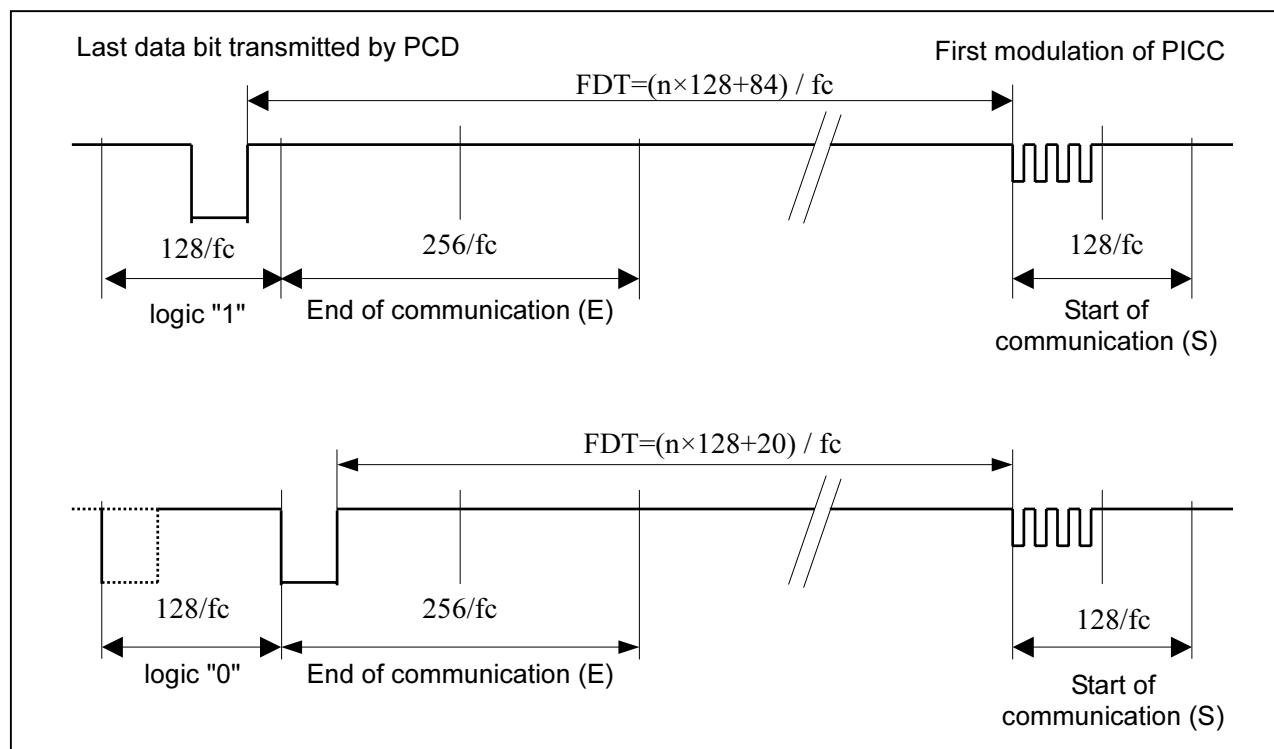


Fig. 12.1-1 Frame Delay Time PCD to PICC

"Table 12.1-1 Frame Delay Time PCD to PICC" defines values for n and FDT depending on the command type and the logic state of the last transmitted data bit in this command.

Table 12.1-1 Frame Delay Time PCD to PICC

command type	n (Integer value)	FDT	
		last bit = (1)b	last bit = (0)b
REQA Command WUPA Command ANTICOLLISION Command SELECT Command	9	$1236 / f_c$	$1172 / f_c$
All other commands	$\geq 9$	$(n \times 128 + 84) / f_c$	$(n \times 128 + 20) / f_c$

The value n=9 means that all PICCs in the field shall respond in a synchronous way which is needed for anticollision.

For all other commands the PICC shall ensure that the first modulation edge within the start bit is aligned to the bit grid defined in "Fig. 12.1-1 Frame Delay Time PCD to PICC".

## (2) Extended Specifications

None

## (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.1.1.3 Frame Delay Time PICC to PCD

#### (1) Basic Specifications

This is the time between the last modulation transmitted by the PICC and the first pause transmitted by the PCD and shall be at least  $1172/f_c$ .

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

#### 12.1.1.4 Request Guard Time

##### (1) Basic Specifications

Request Guard Time is defined as the minimum time between the start bits of two consecutive REQA commands. It has the value  $7000/f_c$ .

##### (2) Extended Specifications

None

##### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.1.1.5 Frame Formats

#### (1) Basic Specifications

The following frame types are defined:

- short frames for commands defined in "Fig. 12.1-2 Short Frame"
- standard frames for regular commands;
- bit oriented anticollision frame for anticollision command.

#### (a) Short Frame

A short frame is used to initiate communication and consists of, in the following order:

- start of communication;
- 7 data bits transmitted LSB first (for coding see "Fig. 12-1-2 Short Frame").
- end of communication

No parity bit us added.

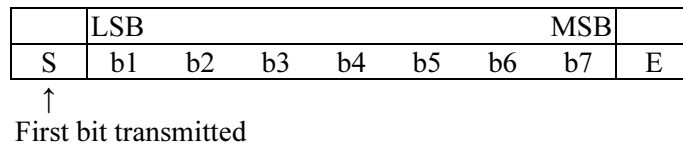


Fig. 12.1-2 Short Frame

## (b) Standard Frame

Standard frames are used for data exchange and consist of :

- start of communication;
- $n \times (8 \text{ data bits} + \text{odd parity bit})$ , with  $n \geq 1$ . The LSB of each byte is transmitted first. Each byte is followed by an odd parity bit. The parity bit P is set such that the number of 1s is odd in (b1 to b8, P);
- Frame end bit
- end of communication.

The composition of standard frames is shown in "Fig. 12.1-3 Standard Frame".

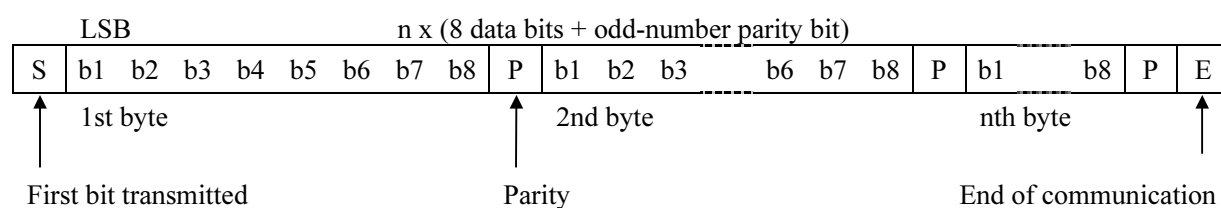


Fig. 12.1-3 Standard Frame

## (c) Bit oriented anticollision frame

A collision is detected when at least two PICCs transmit different bit patterns to the PCD. In this case the carrier is modulated with the subcarrier for the whole bit duration for at least one bit.

Bit oriented anticollision frames shall only be used during bit frame anticollision loops and are standard frames with a length of 7 bytes, split into two parts:

part 1 for transmission from PCD to PICC;

part 2 for transmission from PICC to PCD.

- For the length of part1 and part2, the following rules shall apply:

- rule1: The sum of data bits shall be 56;
- rule 2: The minimum length of part 1 shall be 16 data bits;
- rule 3: The maximum length of part 1 shall be 55 data bits.

Consequently, the minimum length of part 2 shall be 1 data bit and the maximum length shall be 40 data bits.

Since the split can occur at any bit position within a byte, two cases are defined:

- case FULL BYTE: Split after a complete byte. A parity bit is added after the last data bit of part 1;
- case SPLIT BYTE: split within a byte. No parity bit is added after the last data bit of part 1.

The following examples for case FULL BYTE (Fig. 12.1-4 "Bit organization and transmission of bit oriented anticollision frame, case FULL BYTE") and case SPLIT BYTE (Fig. 12.1-5 "Bit organization and transmission of bit oriented anticollision frame, case SPLIT BYTE") define the bit organization and order of bit transmission.



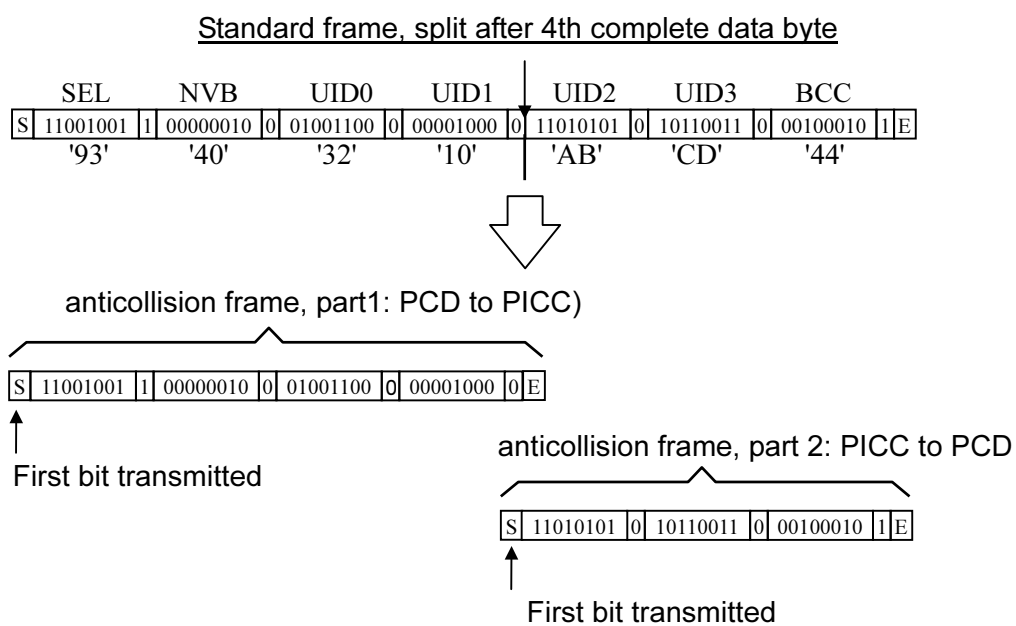


Fig. 12.1-4 Bit organization and transmission of bit oriented anticollision frame, case FULL BYTE

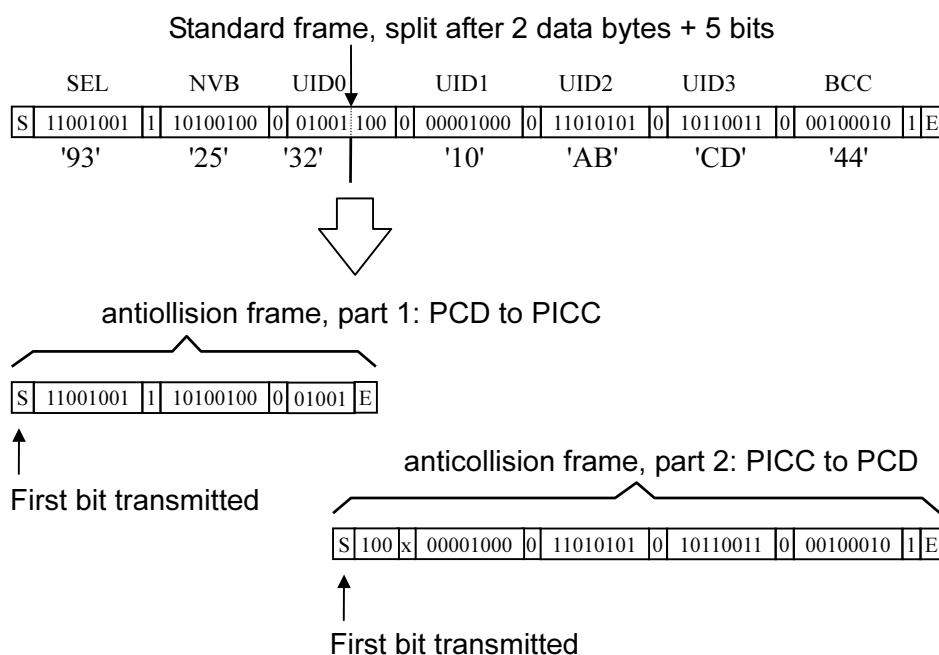


Fig. 12.1-5 Bit organization and transmission of bit oriented anticollision frame, case SPLIT BYTE

For a SPLIT BYTE, the first parity bit of part 2 shall be ignored by the PCD.

(2) Extended Specifications

None

(3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.1.1.6 CRC\_A

#### (1) Basic Specifications

The frame CRC\_A is a function of k data bits, which consist of all the data bits in the frame, excluding parity bits, S and E, and the CRC\_A itself. Since data is encoded in bytes, the number of bits k is a multiple of 8. For error checking, the two CRC\_A bytes are sent in the standard frame, after the bytes and before the E. The CRC\_A is as defined in ISO/IEC 13239, but the initial register content register content shall be '6363' and the register content shall not be inverted after calculation.

For example refer to "12.4 CRC\_A and CRC\_B Encoding".

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

## 12.1.2 PICC States

### (1) Basic Specifications

The following sections provide descriptions of the states for a PICC of Type A specific to the bit collision detection protocol.

"Fig. 12.1-6 PICC Type A state diagram" takes all possible state transitions caused by commands of this chapter into account.

PICCs react to valid received frames only. No response is sent when transmission errors are detected.

The following symbols apply for the state diagram shown in "Fig. 12.1-6 PICC Type A state diagram".

- REQA REQA command
- WUPA WUPA command
- AC ANTICOLLISION Command (match UID)
- nAC ANTICOLLISION Command (not matched UID)
- SEL SELECT Command (matched UID)
- nSEL SELECT Command (not matched UID)
- HLTA HLTA command
- DESEL DESELECT Command, defined in "13. Transmission Protocol".
- Error Transmission error detected

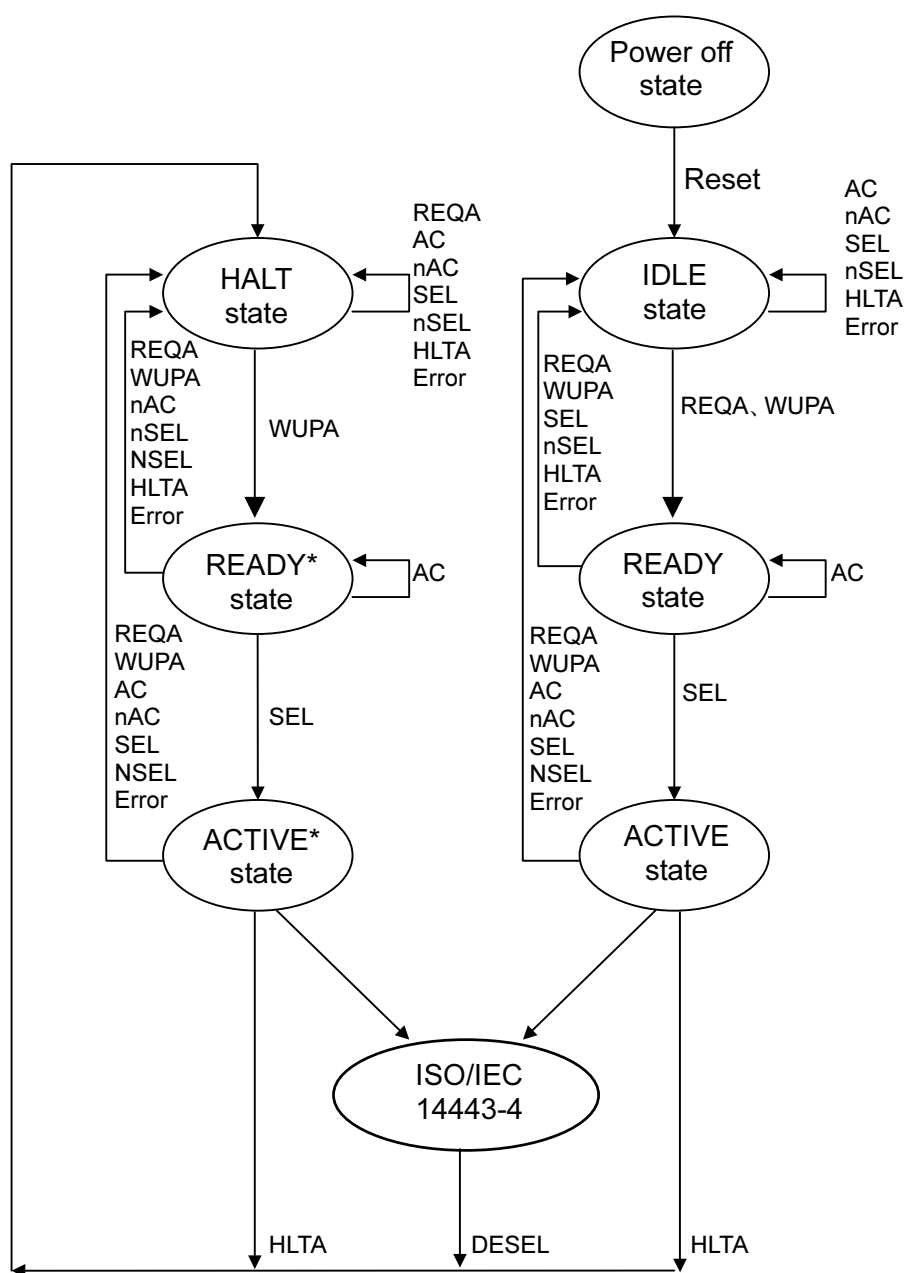


Fig. 12.1-6 PICC Type A State Diagram

PICCs being compliant with the specifications of this chapter but not using the specifications of "13. Transmission Protocol" may leave the ACTIVE or ACTIVE\* State by proprietary commands.

(2) Extended Specifications

None

(3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.1.2.1 Power-OFF State

#### (1) Basic Specifications

- Description:  
In the POWER-OFF State, the PICC is not powered due to a lack of carrier energy.
- State exit conditions and transitions:  
If the PICC is in an energizing magnetic field greater than  $H_{min}$  (see "8. Power Transfer"), it shall enter is IDLE State within a delay not greater than defined in "11. Polling").

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.1.2.2 IDLE State

#### (1) Basic Specifications

- Description

In the IDLE State, the PICC is powered. It listens for commands and shall recognized request commands (REQA) and wakeup commands (WUPA).

- State exit conditions and transitions:

The PICC enters the Ready State after it has received a valid REQA or WUPA Command and transmitted its response (ATQA).

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.



### 12.1.2.3 READY State

#### (1) Basic Specifications

- Description

In the READY State, either the bit frame anticollision or a proprietary anticollision method can be applied (see "12.5 Type A Timeslot - Initialization and Anticollision"). Cascade levels are handled inside this state to get the complete UID.

- State exit conditions and transitions:

The PICC enters the ACTIVE State when it is selected with its complete UID.

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

#### 12.1.2.4 ACTIVE State

##### (1) Basic Specifications

- Description  
In the ACTIVE State, the PICC listens to any higher layer message.
- State exit conditions and transitions:  
The PICC enters the HALT State when a valid halt command (HLTA) is received.
- NOTE  
In the higher layer protocol, specific commands may be defined to return the PICC to its HALT State.

##### (2) Extended Specifications

None

##### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

#### 12.1.2.5 HALT State

##### (1) Basic Specifications

- Description:  
In the HALT State, the PICC shall respond only to a WUPA Command that will make enter into the READY\* state.
- State exit conditions and transitions:  
The PICC enters the READY\* State after it has received a valid WUPA Command and transmitted its ATQA.

##### (2) Extended Specifications

None

##### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.1.2.6 READY\* State

#### (1) Basic Specifications

- Description

The READY\* State is similar to the READY State, either the bit frame anticollision or a proprietary anticollision method can be applied (see "12.5 Type A Timeslot - Initialization and Anticollision"). Cascade levels are handled inside this state to get complete UID.

- State exit conditions and transitions:

The PICC enters the ACTIVE \*State when it is selected with its complete UID.

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.1.2.7 ACTIVE\* State

#### (1) Basic Specifications

- Description  
The ACTIVE\* State is similar to the ACTIVE State, the PICC is selected and listens to any higher layer message.
- State exit conditions and transitions:  
The PICC enters the HALT State when a valid halt command (HLTA) is received.

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.1.3 Command Set

#### (1) Basic Specifications

The Commands used by the PCD to manage communication with several PICCs are:

- Request command (REQA)
- Wakeup command (WUPA)
- Anticollision command (ANTICOLLISION)
- Select command (SELECT)
- Halt command (HLTA)

The commands use the byte and frame formats described in "12.1.1 Frame Formats and Timing".

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.1.3.1 REQA and WUPA Command

#### (1) Basic Specifications

The request (REQA) and wakeup (WUPA) Commands are sent by the PCD to probe the field for PICCs of Type A. They are transmitted within a short frame.

See "Fig. 12.1-6 PICC Type A State Diagram" to check in which cases PICC actually have to answer to these respective commands. Particularly the WUPA Command is sent by the the PCD to put PICCs which have entered the HALT State back into the READY\* State. They shall then participate in furture anticollision and selection procedures.

"Table 12.1-2 Coding of Short Frame" shows the coding of REQA and WUPA Commands which use the Short frame format.

Table 12.1-2 Coding of Short Frame

b7	b6	b5	b4	b3	b2	b1	Description
0	1	0	0	1	1	0	'26' = REQA command
1	0	1	0	0	1	0	'52' = WUPA command
0	1	1	0	1	0	1	'35' = Time slot type (See "12.5 Type A Timeslot - Initialization and Anticollision")
1	0	0	x	x	x	x	'40' to '4F' = Proprietary
1	1	1	1	x	x	x	'78' to '7F' = Proprietary
all other values							RFU

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.1.3.2 ANTICOLLISION and SELECT Command

#### (1) Basic Specifications

These commands are used during and anticollission loop (see "Fig. 12.1-4 Bit organization and transmission of bit oriented anticollision frame, case FULL BYTE" and "Fig. 12.1-5 Bit organization and transmission of bit oriented anticollision frame, case SPLIT BYTE").

The ANTICOLLISION and SELCT Command consists of:

- select code SEL (1 byte);
- number of valid bits NVB (1 byte, for coding see Table 7);
- 0 to 40 data bits of UID CLn according to the value of NVB.

SEL specifies the cascade level CLn. Refer to "12.1.4.3 (c) Coding of NVB (Number of Valid Bits)" for information of encoding of NVB.

The ANTICOLLISION Command is transmitted within bit oriented anticollision frame. The SELECT Command is transmitted within standard frame

As long as NVB does not specify 40 valid bits, the command is called ANTICOLLISION Command, where the PICC remains in READY or READY\* State.

If NVB specifies 40 data bits of UID CLn (NVB='70'), a CRC\_A shall be appended. This command is called SELECT Command. If the PICC has transmitted the complete UID, it transits from READY State to ACTIVE State or from READY\* State to ACTIVE\* State and indicates in its SAK response that UID is complete. Otherwise, the PICC remains in READY or READY\*State and the PCD shall initiate a new anticollision loop with increased cascade level.

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.



### 12.1.3.3 Halt Command

#### (1) Basic Specifications

The HLTA Command consists of two bytes followed by CRC\_A and shall be transmitted within Standard Frame.

The details of the frame of the halt command are shown in "Fig. 12.1-7 Standard Frame Containing HLTA Command".

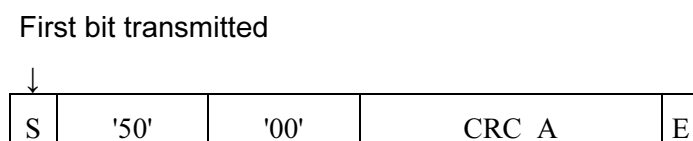


Fig. 12.1-7 Standard Frame Containing HLTA Command

If the PICC responds with any modulation during a period of 1ms after the end of the frame containing the HLTA Command, this response shall be interpreted as 'not acknowledge'.

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

#### 12.1.4 Select Sequence

The purpose of the select sequence is to get the UID from one PICC and to select this PICC for further communication.

##### 12.1.4.1 Select Sequence Flowchart

###### (1) Basic Specifications

A select sequence flowchart is shown in "Fig. 12.1-8 Initialization and Anticollision Flowchart for PCD".

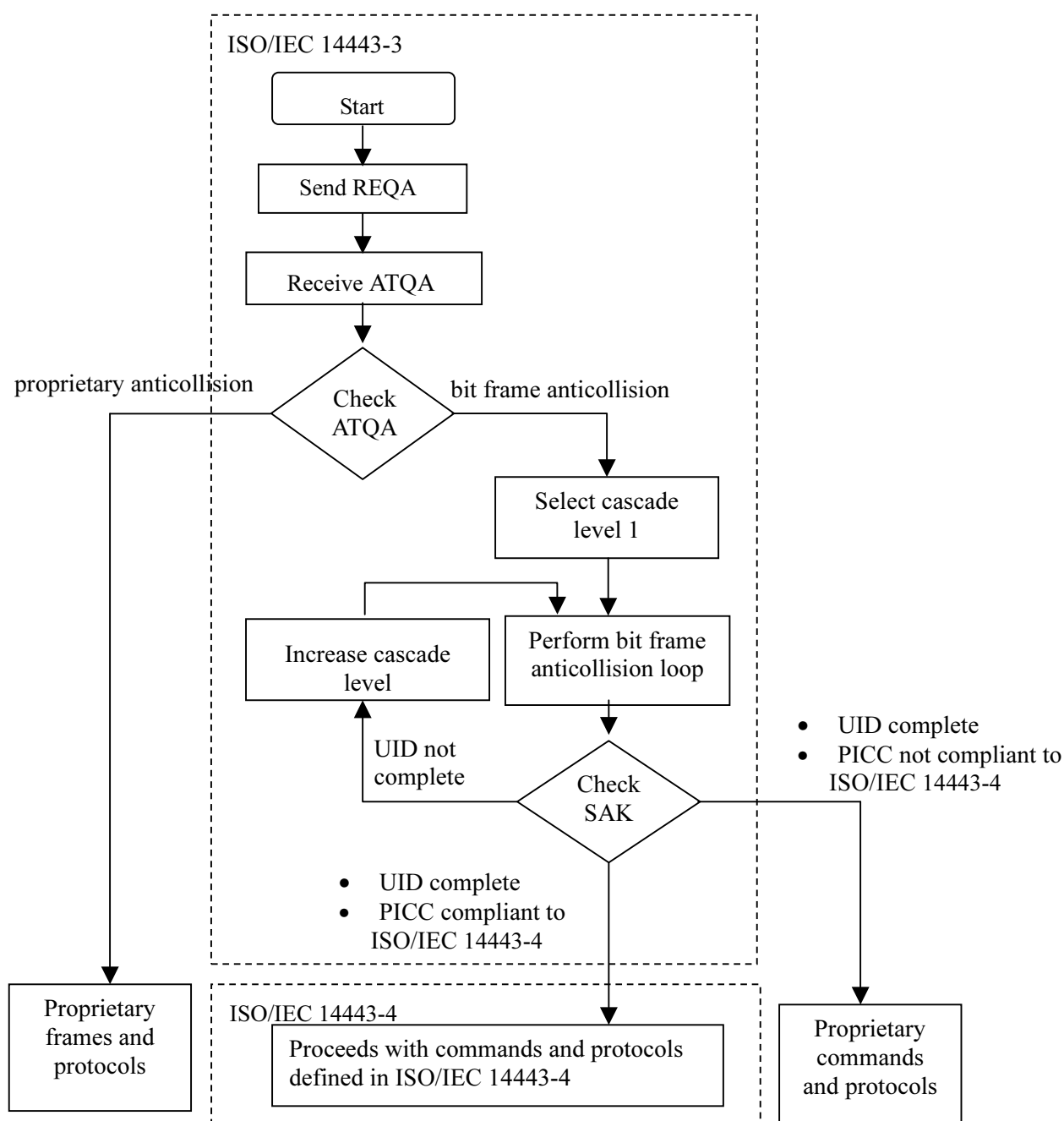


Fig. 12.1-8 Initialization and Anticollision Flowchart for PCD

(2) Extended Specifications

None

(3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.1.4.2 ATQA-Answer To Request

#### (1) Basic Specifications

After a REQA Command is transmitted by the PCD, all PICCs in the IDLE State shall respond synchronously with answer to request signal (ATQA).

After a WUPA Command is transmitted by the PCD, all PICCs in the IDLE or HALT State shall respond synchronously with answer to request signal (ATQA).

The PCD shall detect any collision that may occur when multiple PICCs respond.  
An example is given in "12.3 Communication Example Type A".

#### (a) Coding of ATQA

Encoding of an answer to request signal (ATQA) is shown in "Table 12.1-3 Coding of ATQA".

Table 12.1-3 Coding of ATQA

MSB								LSB							
b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1
(0000)b Other values are RFU				Proprietary coding				UID size bit frame		R F U	Bit frame anticollision				

## (b) Coding rules for bit frame anticollision

- Rule 1: Rule 1: Bits b7 and b8 code the UID size (single, double or triple, see "Table 12.1-4 Coding of b7, b8 for Bit Frame Anticollision").
- Rule 2: One out of the five bits b1, b2, b3, b4 or b5 shall be set to (1)b to indicate bit frame anticollision (see "Table 12.1-5 Coding of b1-b5 for Bit Frame Anticollision").

NOTE Bit9 to bit 12 indicate additional and proprietary methods.

Table 12.1-4 Coding of b7, b8 for Bit Frame Anticollision

b8	b7	Meaning
0	0	UID size: Single
0	1	UID size: Double
1	0	UID size: Triple
1	1	RFU

Table 12.1-5 Coding of b1-b5 for Bit Frame Anticollision

b5	b4	b3	b2	b1	Meaning
1	0	0	0	0	Bit frame anticollision
0	1	0	0	0	Bit frame anticollision
0	0	1	0	0	Bit frame anticollision
0	0	0	1	0	Bit frame anticollision
0	0	0	0	1	Bit frame anticollision
Other values					RFU

## (0) Extended Specifications

None

## (1) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.1.4.3 Anticollision and Select

#### (1) Basic Specifications

##### (a) Anticollision loop within each cascade level

The following algorithm shall apply to the anticollision loop:

- 1) The PCD shall assign SEL with the code for the selected anticollision type and cascade level.
- 2) The PCD shall assign NVB with the value of '20'.  
Note: This value defines that the PCD will transmit no part of UID CLn. Consequently this command forces all PICCs in the field to respond with their complete UID CLn.
- 3) The PCD shall transmit SEL and NVB.
- 4) All PICCs in the field shall respond with their complete UID CLn.
- 5) Assuming the PICCs in the field have unique serial numbers, then if more than one PICC responds, a collision occurs. If no collision occurs, steps 6) to 10) shall be skipped.
- 6) The PCD shall recognize the position of the first collision.
- 7) The PCD shall assign NVB with a value that specifies the number of valid bits of UID CLn. The valid bits shall be part of the UID CLn that was received before a collision occurred followed by a (0)b or (1)b, decided by the PCD. A typical implementation adds a (1)b.
- 8) The PCD shall transmit SEL and NVB, followed by the valid bits.
- 9) Only PICCs of which the part of UID CLn is equal to the Valid bits transmitted by the PCD shall transmit their remaining bits of the UID CLn.
- 10) If further collisions occur, steps 6) to 9) shall be repeated. The maximum number of loops will be 32.

- 11) If no further collision occurs, the PCD shall assign NVB with the value of '70'.  
Note: This value defines that the PCD will transmit the complete UID CLn.
- 12) The PCD shall transmit SEL and NVB, followed by all 40 bits of UID CLn, followed by CRC\_A checksum.
- 13) The PICC which UID CLn matches the 40 bits shall respond with its SAK.
- 14) If the UID is complete, the PICC shall transmit SAK with cleared cascade bit and shall transit from READY State to ACTIVE State to ACTIVE\* State..
- 15) The PCD shall check if the cascade bit of SAK is set to decide whether further anticollision loops with increased cascade level shall follow.

If the UID of a PICC is complete and known by the PCD, the PCD may skip step 2- step 10 to select this PICC without performing the anticollision loop.

The above procedure from 1) to 13) is illustrated in "Fig. 12.1-9 Anticollision Loop, Frowchart for PCD".



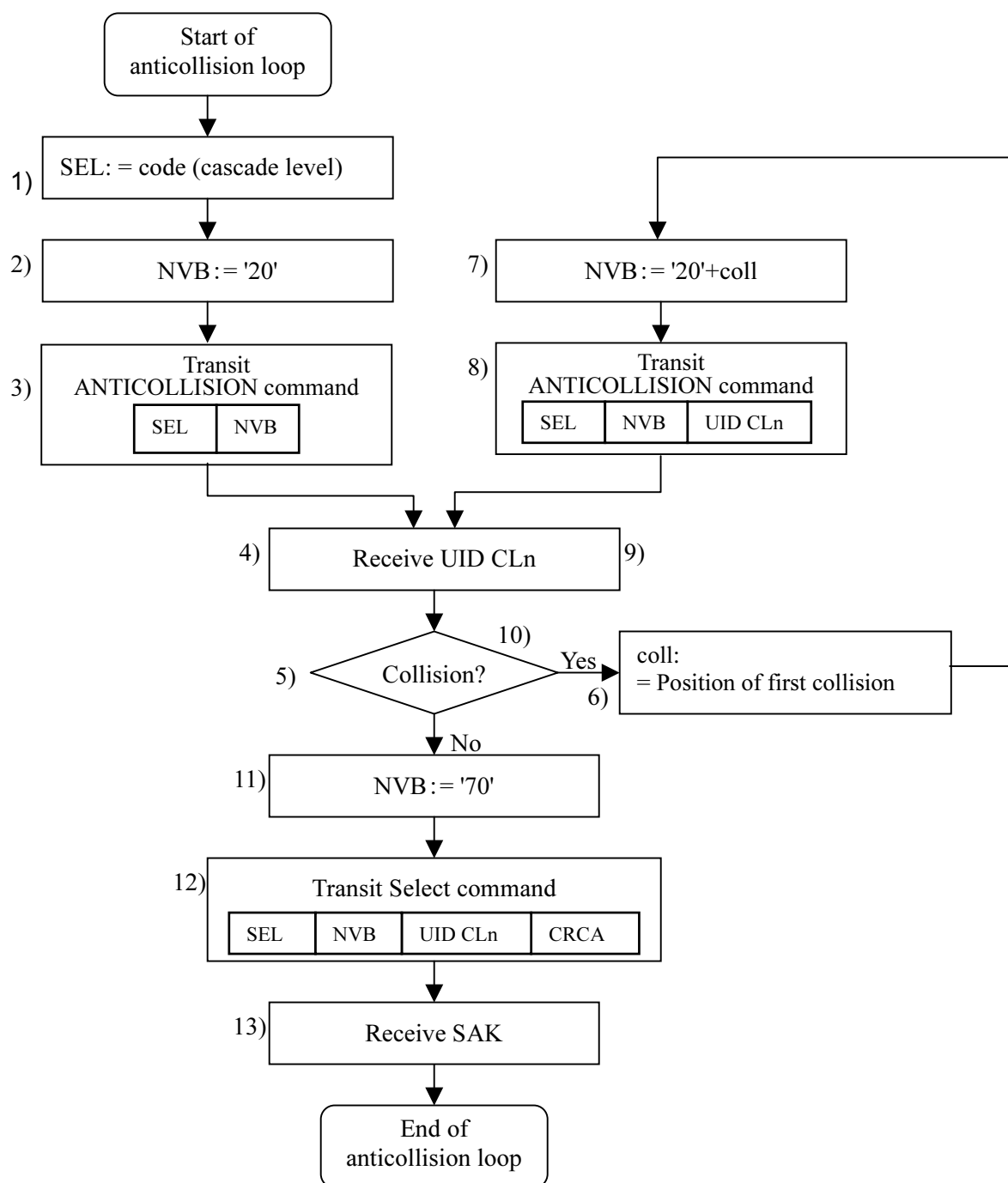


Fig. 12.1-9 Anticollision Loop, Flowchart for PCD

## (b) Coding of SEL (Select code)

- Length: 1 byte
- Possible values: '93', '95', '97'

Details are shown in "Table 12.1-6 Coding of SEL ".

Table 12.1-6 Coding of SEL

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
1	0	0	1	0	0	1	1	'93': Select cascade level 1
1	0	0	1	0	1	0	1	'95': Select cascade level 2
1	0	0	1	0	1	1	1	'97': Select cascade level 3
1	0	0	1	Other values				RFU

## (c) Coding of NVB (Number of Valid Bits)

- Length: 1 byte

The upper 4 bits are called "Byte count" and specify the integer part of the number of all valid data bits transmitted by the PCD (including SEL and NVB) divided by 8. Consequently, the minimum value of "Byte count" is 2 and the maximum value is 7.

The lower 4 bits are called "bit count" and specify the number of all valid data bits transmitted by the PCD (including SEL and NVB) modulo 8.

The details are shown in "Table 12.1-7 Coding of NVB".

Table 12.1-7 Coding of NVB

b8	b7	b6	b5	Meaning
0	0	1	0	Byte count = 2
0	0	1	1	Byte count = 3
0	1	0	0	Byte count = 4
0	1	0	1	Byte count = 5
0	1	1	0	Byte count = 6
0	1	1	1	Byte count = 7

b4	b3	b2	b1	Meaning
0	0	0	0	bit count = 0
0	0	0	1	bit count = 1
0	0	1	0	bit count = 2
0	0	1	1	bit count = 3
0	1	0	0	bit count = 4
0	1	0	1	bit count = 5
0	1	1	0	bit count = 6
0	1	1	1	bit count = 7

## (d) Coding of SAK (Select acknowledge)

SAK is transmitted by the PICC when NVB has specified 40 valid data bits and when all these data bits math with UID CLn. The composition of SAK is shown in "Fig. 12.1-10 Select acknowledge (SAK)".

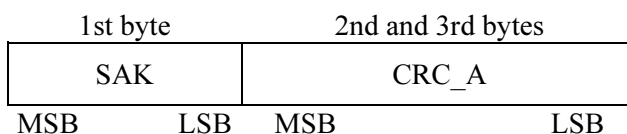


Fig. 12.1-10 Select Acknowledge (SAK)

PCD checks b3 in order to investigate whether or not the UID is complete. The coding of bits b3 (cascade bit) and b6 is given in "Table 12.1-8 Coding of SAK".

Table 12.1-8 Coding of SAK

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
x	x	x	x	x	1	x	x	Cascade bit set: UID not complete
x	x	1	x	x	0	x	x	UID complete. PICC compliant with ISO/IEC 14443-4
x	x	0	x	x	0	x	x	UID complete. PICC not compliant with ISO/IEC 14443-4

If the UID is not complete, the PICC remains in the READY state or READY\* state. The PCD advances the cascade level by 1 and repeats the anticollision loop.

In the case of the UID is complete, the PICC clears the cascade bit, returns SAK and changes from the READY state to the ACTIVE state or from the READY\* state to the ACTIVE\* state. If the PICC complies with ISO/IEC 14443-4, the PICC sets b6 of SAK.

(2) Extended Specifications

None

(3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

#### 12.1.4.4 UID Contents and Cascade Levels

##### (1) Basic Specifications

The UID consists of 4, 7 or 10 UID bytes. Consequently, the PICC shall handle up to 3 cascade levels to get all UID bytes. Within each cascade level, a part of UID shall be transmitted to the PCD. According to the cascade level, three types of UID size are defined. This UID size shall be consistent with "Table 12.1-9 UID size".

Table 12.1-9 UID Size

Cascade level	UID size	Number of UID bytes
1	Single	4
2	Double	7
3	Triple	10

The contents of the UID are specified as shown below.

- UID CL<sub>n</sub> UID portion at cascade level n ( $3 \geq n \geq 1$ )
- UID<sub>n</sub> nth ( $n \geq 0$ ) byte of UID
- BCC Exclusive OR of first 4 bytes among checked bytes of UID CL<sub>n</sub>
- CT Cascade tag (value is '88')

The UID is a fixed unique number or a random number which is dynamically generated by the PICC. The first byte (uid0) of the UID assigns the content of the following bytes of the UID.

The contents of UID during single operation are shown in "Table 12.1-10 Single size of UIDs".

Table 12.1-10 Single Size of UIDs

uid0	Description
'08'	uid1 to uid3 is a random number which is dynamically generated
'x0' - 'x7'	proprietary fixed number
'x9' - 'xE'	
'18' - 'F8'	RFU
'xF'	

The value '88' of the cascade tag CT shall not be used for uid0 in single size UID

The contents of double size and triple size UIDs are shown in "Table 12.1-11 Double and triple size UIDs".

Table 12.1-11 Double and Triple Size UIDs

uid0	Description
Manufacturer ID according to ISO/IEC 7816-6/AM1 (*)	Each manufacturer is responsible for making characteristic values other than uid0 characteristic.

(\*) The value '81' to 'FE', which are marked for 'Private use' in ISO/IEC 7816-6/AM1 shall not be allowed in this context.

The method of using the cascade levels is shown in "Fig. 12.1-11 Usage of Cascade Levels".

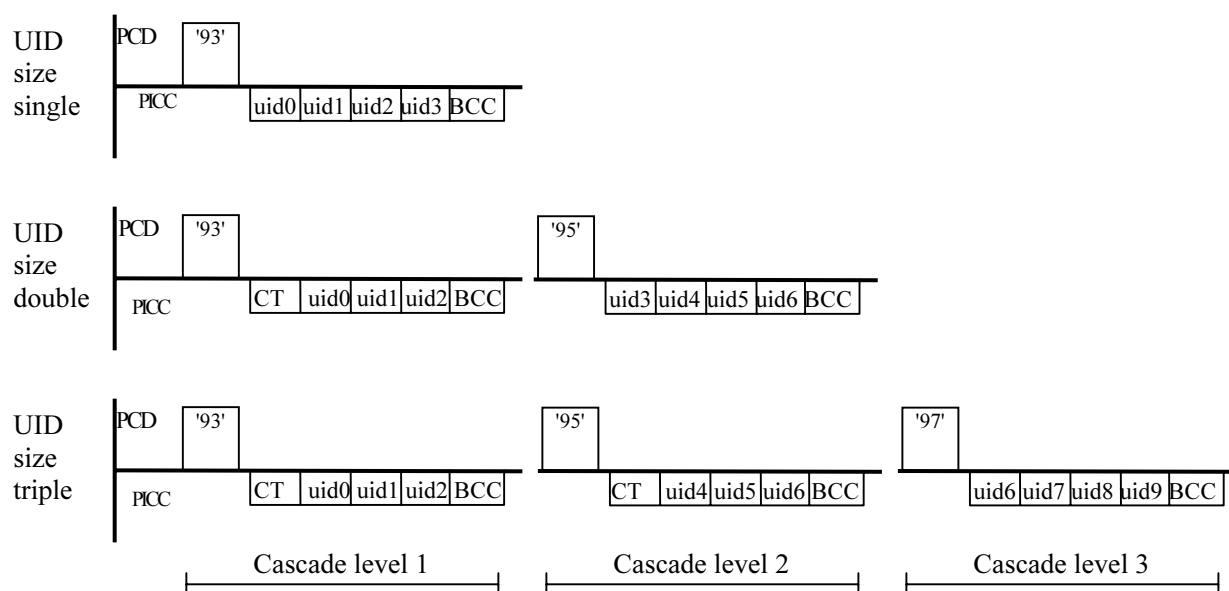


Fig. 12.1-11 Usage of Cascade Levels

NOTE: The purpose of the cascade tag is to force a collision with PICCs that have a smaller UID size. Consequently, UID0 and UID3 must not have the same values as the value of the cascade tag.

The procedure by which the PCD obtains a complete UID is as shown below.

- Step 1: The PCD selects cascade level1
- Step 2: The anticollision loop shall be performed
- Step 3: The PCD shall check the cascade bit of SAK
- Step 4: If the cascade bit is set, the PCD shall increase the cascade level and initiate a new anticollision loop

## (2) Extended Specifications

None

## (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.



## 12.2 Type B - Initialization and Anticollision

This section describes the initialization and collision detection protocol application for PICCs of Type B.

### 12.2.1 Character, Frame Format and Timing

#### (1) Basic Specifications

This section defines the character, frame format and timing used during communication initialization and anticollision for PISs of Type B. For bit representation and coding refer to ISO/IEC 14443-2.

#### (2) Extended Specifications

None

#### (3) References

None

### 12.2.1.1 Character Transmission Format

#### (1) Basic Specifications

Bytes are transmitted and received between PICCs and a PCD by characters, the format of which during the Anticollision sequence is as follows:

- 1 start bit at logic "0";
- 8 data bits transmitted, LSB first;
- 1 stop bit at logic "1";

The transmission of one byte is performed with a character requiring 10 etu as illustrated in "Fig. 12.2-1 Character Format".

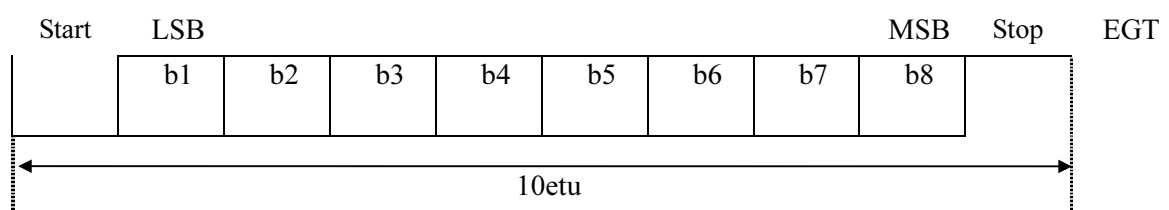


Fig. 12.2-1 Character Format

Bit boundaries within a character shall occur between  $(n-0.125)$  etu and  $(n+0.125)$  etu where  $n$  is the number of bit boundaries after the start bit falling edge ( $1 \leq n \leq 9$ )

#### (2) Extended Specifications

None

#### (3) References

None

### 12.2.1.2 Character Separation

#### (1) Basic Specifications

A character is separated from the next one by the extra guard time EGT.

The EGT between 2 consecutive characters sent by the PCD to the PICC shall be between 0 and 57  $\mu\text{s}$ .

The EGT between 2 consecutive characters sent by the PCD to the PICC shall be between 0 and 19  $\mu\text{s}$ .

#### (2) Extended Specifications

None

#### (3) References

None

### 12.2.1.3 Frame Format

#### (1) Basic Specifications

PCDs and PICCs shall send characters as frames. The frame is normally delimited by SOF and by EOF.

The frame organization used by PCD and PICC is shown in "Fig. 12.2-2 Frame Format".

SOF	Character	EOF
-----	-----------	-----

Fig. 12.2-2 Frame Format

#### (2) Extended Specifications

None

#### (3) References

None

### 12.2.1.4 Start Of Frame (SOF)

#### (1) Basic Specifications

SOF is composed of:

- one falling edge;
- followed by 10 etu with a logic "0";
- followed by one single rising edge located anywhere within the following etu;
- followed by at least 2 etu (but no more than 3 etu) with logic "1".

The composition of SOF is shown in "Fig. 12.2-3 SOF".

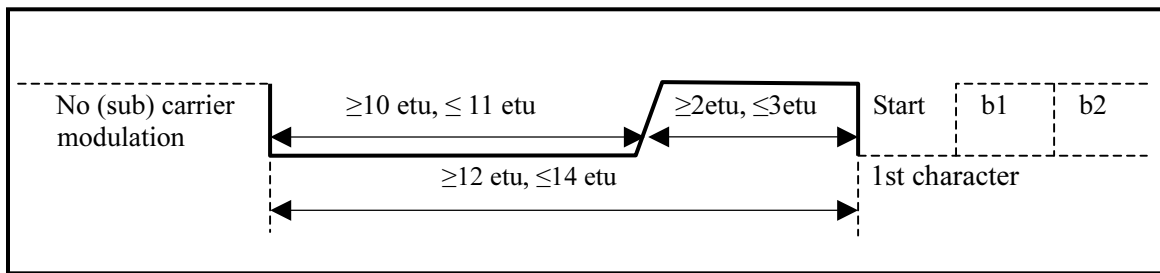


Fig. 12.2-3 SOF

#### (2) Extended Specifications

None

#### (3) References

None

### 12.2.1.5 End Of Frame (EOF)

#### (1) Basic Specifications

EOF is composed of:

- one falling edge;
- followed by 10 etu with a logical "0";
- followed by one single rising edge located anywhere within the following etu.

The composition of EOF is shown in "Fig. 12.2-4 EOF".

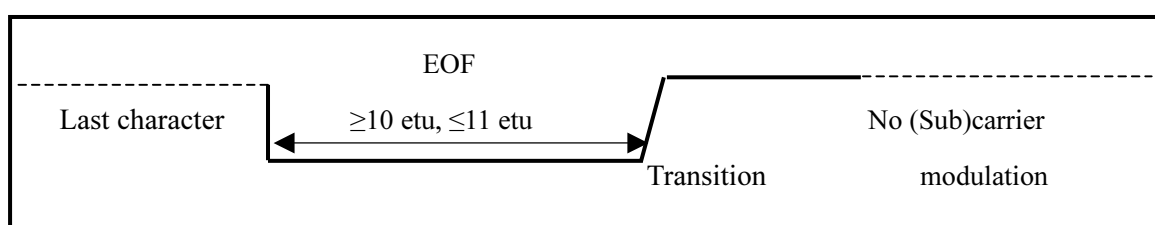


Fig. 12.2-4 EOF

Note: The probability of receiving a false EOF is low and corresponds to the transmission of a '00' character with a wrong reception of the stop bit.

#### (2) Extended Specifications

None

#### (3) References

None

12.2.1.6 Subcarrier from PICC to PCD and SOF

(1) Basic Specifications

PICC start of communication after a PCD data transmission shall respect the timing defined in "Fig. 12.2-5 PICC subcarrier SOF ".

The default minimum values of TR0 and TR1 are defined in ISO/IEC 14443-2 and may be reduced by the PCD, (see "12.2.10 ATTRIB Command").

The maximum value of TR0 is 256/fs for ATQB only and  $(256/fs) \cdot 2^{FWI}$  for all other frames. The maximum value of TR1 is 200/fs.

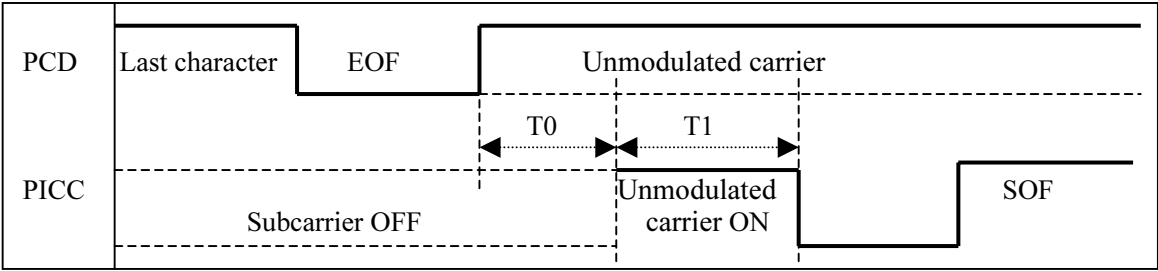


Fig. 12.2-5 PICC subcarrier SOF

A PICC may turn on the subcarrier only if it intends to begin transmitting information.

(2) Extended Specifications

None

(3) References

None

### 12.2.1.7 Subcarrier from PICC to PCD and EOF

#### (1) Basic Specifications

PCD start of communication after a PICC data transmission and EOF shall EOF shall respect the timing defined in "Fig. 12.2-6 PICC to PCD EOF".

The PICC shall turn off its subcarrier after the transmission of the EOF. The subcarrier signal shall:

- not be stopped before the end of the EOF;
- be stopped no later than  $et_u$  after the end of the EOF.

The minimum delay between the PICC EOF start (falling edge) and the PCD SOF start (falling edge) is  $10 et_u + 32/fs$ .

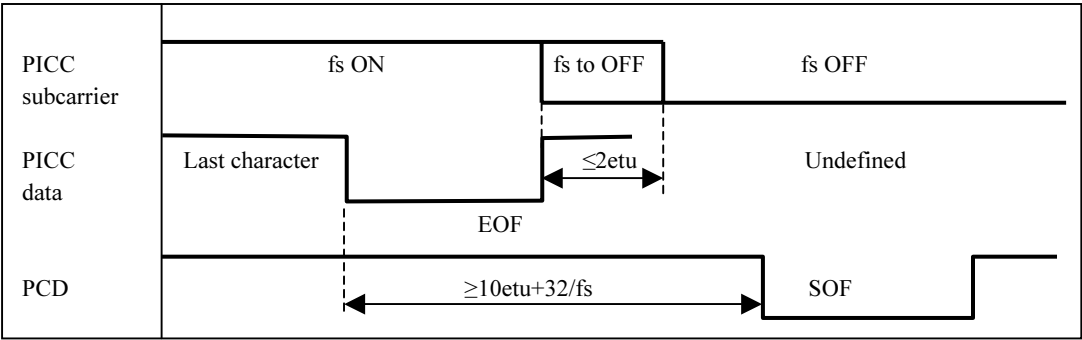


Fig. 12.2-6 PICC to PCD EOF

#### (2) Extended Specifications

None

#### (3) References

None



## 12.2.2 Cyclic Redundancy Check Code (CRC\_B)

### (1) Basic Specifications

The frame insertion position of CRC\_B is shown in "Fig. 12.2-7 Frame Insertion Position of CRC\_B".

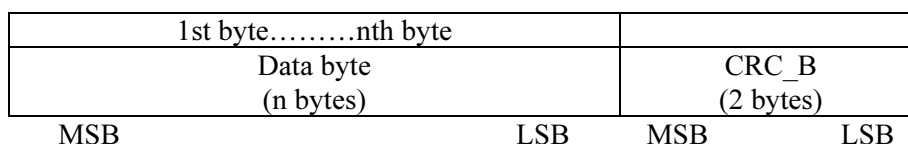


Fig. 12.2-7 Frame Insertion Position of CRC\_B

The frame CRC\_B is a function of k data bits, which consist of all the data bits in the frame, excluding start bits, stop bits, delays between bytes, SOF and EOF, and the CRC\_B itself. Since data is encoded in bytes, the number of bits k is a multiple of 8.

For error checking, the two CRC\_B bytes are included in the frame, after the data bits and before the EOF. The CRC\_B is as defined in ISO/IEC 13239. The initial register content shall be all ones: 'FFFF'.

Encoding examples of CRC\_A and CRC\_B are shown in "12.4 CRC\_A and CRC\_B Encoding".

### (2) Extended Specifications

None

### (3) References

None

### 12.2.3 Anticollision Sequence

#### (1) Basic Specifications

An anticollision sequence is managed by the PCD through a set of commands detailed in this chapter. The PCD is the master of the communication with one or more PICCs. It initiates PICC communication activity by issuing a REQB Command to prompt for PICCs to respond.

During the anticollision sequence it may happen that two or more PICCs respond simultaneously: this is a collision. The command set allows the PCD to handle sequences to separate PICC transmissions in time. The PCD may repeat its anticollision procedure until it finds all PICCs in the operating volume.

Having completed the anticollision sequence, PICC communication will be under control of the PCD, allowing only one PICC to talk at a time.

The collision scheme is based on definition of timeslots in which PICCs are invited to answer with minimum identification data. The number of slots is parameterized in the REQB/WUPB and can vary from one to some integer number. PICC response probability in each timeslot is also controllable. PICCs are allowed to answer only once in the anticollision sequence.

Consequently, even in case of multiple PICCs present in the PCD field, there will probably be a slot in which only one PICC answers and where the PCD is able to capture the identification data. Based on the identification data the PCD is able to establish a communication channel with the identified PICC.

An anticollision sequence allows selection of one or more PICCs for further communication at any time.

The set of commands allows implementation of different anticollision management strategies at the PCD level. This strategy is under the control of the application designer and can include:

- probabilistic (repetitive single slot prompt with response probability less than or equal to 1);
- pseudo-deterministic (multiple slots with scanning of them during the anticollision sequence to have the maximum probability that all present PICCs answer);

#### (2) Extended Specifications

None

#### (3) References

None

## 12.2.4 PICC States Description

### (1) Basic Specifications

An example of a flow chart of the Different states and transition conditions between states is shown in "Fig. 12.2-8 PICC state transition flowchart example".

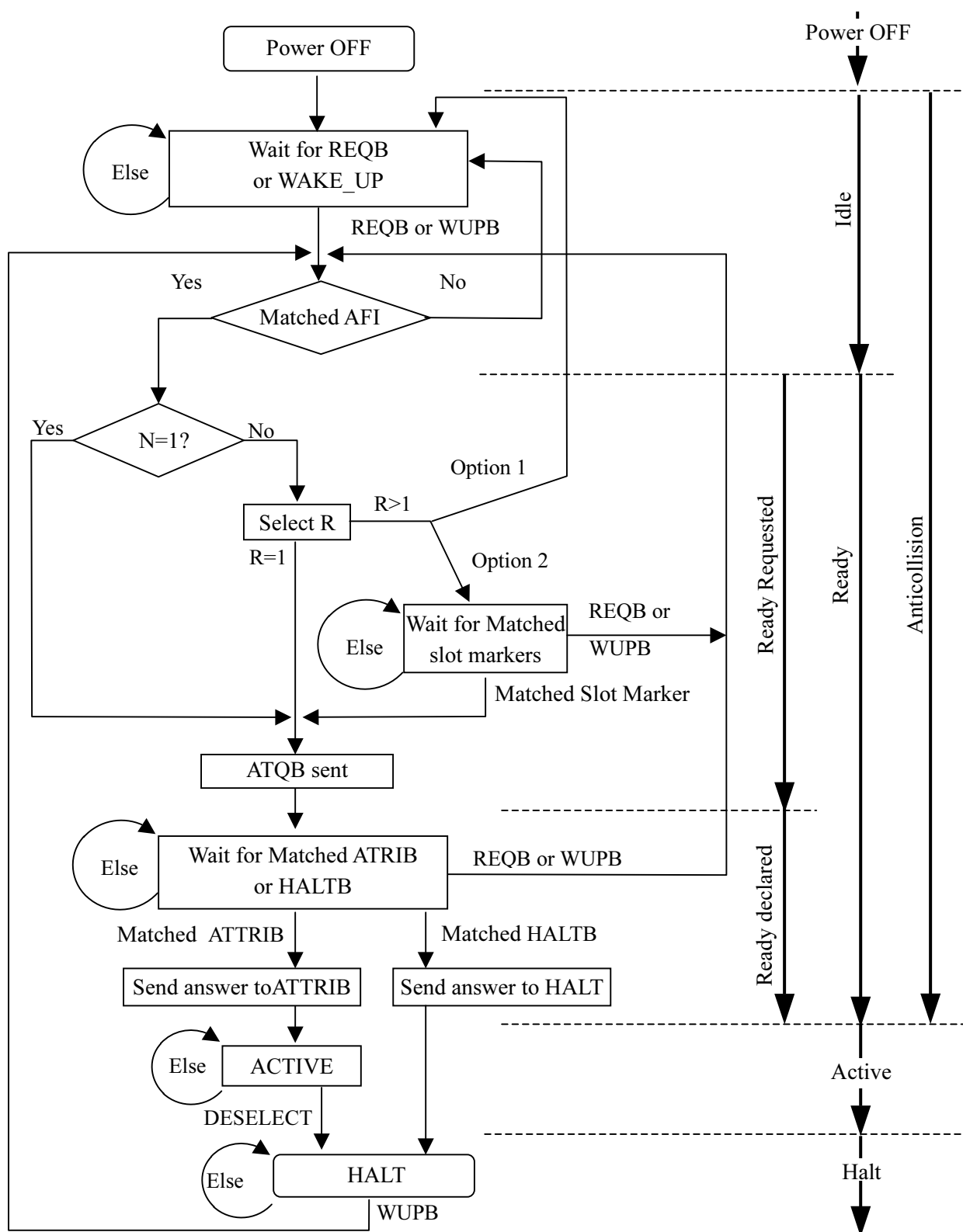


Fig. 12.2-8 PICC state transition flowchart example

- Note 1:

In the Figure, R is a random number chosen by the PICC in the range from 1 to N (refer to "12.2.7.4 Encoding of PARAM" for information on encoding of N).

- Note 2:

In the Figure, OPTION 1: For PICCs not supporting Slot-MARKER Command (Probabilistic approach). OPTION 2: For PICC supporting Slot-MARKER Command (Timeslot approach).

## (2) Extended Specifications

None

## (3) References

In the case of not using Slot\_MARKER commands, namely in the case of using the Timeslot approach, processing is performed as shown below. However, since this type of processing is not defined in the specifications of ISO/IEC 14443, adequate considerations are to be given to the system when using this type of processing.

In "Fig. 12.2-8 PICC State Transition Flowchart Example", processing to evaluate b5 of the PARAM portion of REQ\_B after evaluating whether or not AFI match, is added.

If b5 = (0)b, processing proceeds to evaluating whether or not N = 1. Subsequent processing is the same as in "Fig. 12.2-8 PICC State Transition Flowchart Example".

If case b5 = (1)b, processing is performed in the order shown below.

- 1) R select
- 2) Wait until slot timing agree
- 3) Send ATQB (subsequent processing is the same as in "Fig. 12.2-8 PICC State Transition Flowchart Example")

The PCD sends a command in which b5 of the PARAM portion of REQ\_B is set to (1)b.

### 12.2.4.1 General Statement for State Description and Transitions

#### (1) Basic Specifications

To any state the following shall apply:

- the PICC shall return to POWER\_OFF State if the RF field disappears.

To any state specific to the anticollision sequence (except ACTIVE State) the following shall apply:

- Default communication parameters as defined in "12.2.1 Character, Frame Format and Timing" shall be used.
- The PICC shall not emit subcarrier except to transmit response frames as specified in the previous sections.
- The PICC will become able to receive commands from the PCD when power is transmitted to the PICC and reset is released.
- If a frame from the PCD is valid (correct CRC\_B), the PICC shall perform the required action and/or response depending on its state as in anticollision commands the first 3 bits of the data in a frame are (101)b (3 first bits of anticollision Prefix byte)
- The PICC shall not answer to any command frame not starting with (101)b.
- The PICC shall only react to valid frames received (no response sent when transmission errors are detected).

#### (2) Extended Specifications

None

#### (3) References

None

#### 12.2.4.2 Power OFF State

##### (1) Basic Specifications

- Definition of State

In the POWER-OFF State, the PICC is not powered due to a lack of carrier energy.

State exit conditions and transitions:

- Conditions for State Transition and Transition Destination

If the PICC is in an energizing magnetic field greater than Hmin (see "8. Power Transfer"), it shall enter its IDLE State within a delay not greater than defined in "11. Polling").

##### (2) Extended Specifications

None

##### (3) References

None

### 12.2.4.3 IDLE State

#### (1) Basic Specifications

- Definition of State

In the IDLE State, the PICC is powered. It listens for frames and shall recognize REQB and WUPB messages.

- State exit conditions and transitions:

On reception of valid REQB or WUPB Command frames the PICC moves onto the READY REQUESTED sub-state. (Valid REQB/WUPB means valid with REQB/WUPB Command and matched AFI. See "12.2.7 REQB/WUPB Commands" for details.

#### (2) Extended Specifications

None

#### (3) References

None



#### 12.2.4.4 READY-REQUESTED Sub-state

##### (1) Basic Specifications

- Definition of State

In the READY-REQUIRED sub-state, the PICC is powered and has received a valid REQB or WUPB Commands with a control parameter N. The PICC calculate a random number R which is used to control its subsequent operation as described in "12.2.6 Anticollision Response Rules".

- State exit conditions and transitions:

Refer to "12.2.6 Anticollision Response Rules".

##### (2) Extended Specifications

None

##### (3) References

None

#### 12.2.4.5 READY-DECLARED Sub-state

##### (1) Basic Specifications

###### - Definition of State

In the READY-DECLARED sub-state, the PICC is powered and has sent its ATQB corresponding to the last valid REQB/WUPB message received. It listens to frames and shall recognize REQB/WUPB ATTRIB and HLTB commands.

###### - State exit conditions and transitions:

On reception of a valid ATTRIB Command the PICC shall enter the ACTIVE State if the PUPI in the ATTRIB Command matches the PICC PUPI.

If the PUPI in the ATTRIB Command does not match the PICC PUPI the PICC remains in the READY-DECLARED sub-state.

On reception of a valid REQB/WUPB Command frame the same conditions and transitions apply as on reception of a valid REQB/WUPB Command in the IDLE State.

On reception of a matched HLTB Command the PICC shall enter the HALT State.

##### (2) Extended Specifications

None

##### (3) References

None

#### 12.2.4.6 ACTIVE State

##### (1) Basic Specifications

- Definition of State

The PICC is powered and has entered a higher layer mode since a Card Identifier (CID) has been assigned to this PICC through the ATTRIB Command.

The PICC listens to any higher layer message properly formatted (proper CID and valid CRC\_B)

The PICC shall not emit subcarrier following any frame with invalid CRC\_B or with another CID than the one assigned.

- State exit conditions and transitions:

The PICC enters the HALT State when a valid DESELECT Command frame is received (DESELECT Command is defined in ISO/IEC 14443-4).

- Specific remarks:

Valid REQB/WUPB or Slot-MARKER frames shall not be answered. A valid frame with an ATTRIB Command shall not be answered.

In the higher layer protocol, specific commands may be defined to return the PICC to other states (IDLE or HALT). The PICC may return to these states only following reception of such commands.

##### (2) Extended Specifications

None

##### (3) References

None

#### 12.2.4.7 HALT State

##### (1) Basic Specifications

- Definition of State

The PICC shall respond only to a WUPB Command which brings it back to the IDLE State.

- State exit conditions and transitions:

The PICC returns to the POWER\_OFF State if the RF field disappears.

##### (2) Extended Specifications

None

##### (3) References

None

## 12.2.5 Command Set

### (1) Basic Specifications

Four primitive commands are used to manage multi-node communication channels:

- REQB/WUPB
- Slot\_MARKER
- ATTRIB
- HLTB

These four commands use the bit and byte formats described in detail in "12.2.1 Character and Frame Formats and Time Specifications".

The commands and the response of the PICC to these commands are described in the following sections. Any frame received with a wrong format (wrong frame identifiers or invalid CRC\_B) shall be ignored.

### (2) Extended Specifications

None

### (3) References

The PCD does not send Slot\_MARKER command.

## 12.2.6 Anticollision Response Rules

### (1) Basic Specifications

A PICC which is in the READY-REQUESTED sub-state, after receiving a valid REQB/WUPB Command (Requested AFI=0 or AFI matched with an internal application), shall respond according to the following the rules, where the parameter N has been given in the REQB/WUPB Commands:

- a) If  $N=1$  the PICC shall send an ATQB and shall move to the READY-DECLARED sub-state
- b) If  $N>1$  the PICC shall internally generate a random number R which shall be evenly distributed between 1 to N
  - 1) If  $R=1$  the PICC shall send an ATQB and shall move to the READY-DECLARED sub-state.
  - 2) If  $R>1$  PICCs employing the probabilistic approach shall return to IDLE State; PICCs employing the slot marker approach shall wait until they have received a Slot-MARKER Command with a matched slot number (slot number=R) before sending the ATQB and moving to the READY-DECLARED sub-state.

## (2) Extended Specifications

None

## (3) References

If b5 of the PARAM portion of REQb/WUPb is (0)b, basic specifications are applied, and if it is (1)b, processing is performed as described below.

- a) When  $N = 1$ : The PICC sends ATQB.
- b) When  $N > 1$ : The PICC internally generates a random number  $R$  ( $1 \leq R \leq N$ ).  
The PICC then sends ATQB after waiting for a period corresponding to the value of  $R$ .

The relationship between random number  $R$  (= slot number) and the timing by which ATQB is sent is as shown below.

1) When  $R = 1$ :

The period of 32 etu following completion of EOF of the REQb/WUPb command sent by the PCD shall be the guard time  $t_A$ . Following completion of  $t_A$ , a period of 240 etu ( $t_B$ ) shall be the first slot. The PICC may send ATQB at any arbitrary timing of the first slot. However, the period of the final 10 etu ( $t_C$ ) in  $t_B$  shall be the inter-slot guard time, and the PICC must not send out a subcarrier during this time.

2) When  $R > 1$ :

The period of 240 etu following completion of the  $(R-1)$ st slot shall be the  $R$ th slot. The PICC may send ATQB at any arbitrary timing of the  $R$ th slot. However, the period of the final 10 etu ( $t_C$ ) in  $t_B$  shall be the inter-slot guard time, and the PICC must not send out a subcarrier during this time.

## 12.2.7 REQB/WUPB Command

### (1) Basic Specifications

The REQB and WUPB Commands sent by the PCD are used to probe the field for PICCs of Type B.

In addition WUPB is particularly used to also wake up PICCs which are in HALT Sate.

The number of slots N is included in the command as a parameter to optimize the anti-collision algorithm for a given application. See "Fig. 12.2-8 PICC state Transition Flowchart Example" for detailed description of when the PICC shall respond to these respective commands.

### (2) Extended Specifications

None

### (3) References

None



12.2.7.1 REQB/WUPB Command Format

(1) Basic Specifications

These commands are send out in the form of 5 bytes by the PCD. Refer to "Fig. 12.2-9 REQB/WUPB Command Format" for details.

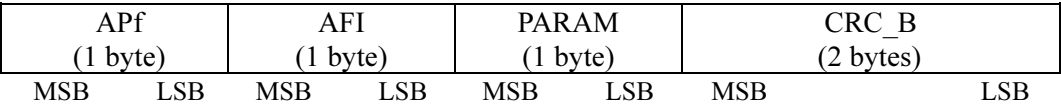


Fig. 12.2-9 REQB/WUPB Command Format

(2) Extended Specifications

None

(3) References

None

### 12.2.7.2 Coding of Anticollision Prefix byte APf

#### (1) Basic Specifications

The Anticollision Prefix byte is APf = '05' = (0000 0101)b.

#### (2) Extended Specifications

None

#### (3) References

None

### 12.2.7.3 Coding of AFI

#### (1) Basic Specifications

AFI (Application Family Identifier) represents the type of application targeted by the PCD and is used to preselect PICCs before the ATQB. Only PICCs with applications of the type indicated by the AFI may answer to a REQB/WUPB Command with AFI different to '00'.

When AFI is '00', all PICCs shall process the REQB/WUPB.

The most significant half byte of AFI is used to code one specific or all application families, as defined in "Table 12.2-1 Coding of AFI". The least significant half byte of AFI is used to code one specific or all application sub-families. Sub-family codes different from 0 are proprietary.

Table 12.2-1 Coding of AFI

AFI upper 4 bits	AFI lower 4 bits	Meaning - PICCs respond from	Example/Note
'0'	'0'	All families and sub-families	No application preselection
X	'0'	All sub-families of family X	Wide application preselection
X	Y	Only the Yth sub-family and family X	
'0'	Y	Proprietary sub-family Y only	
'1'	'0' , Y	Transport	Mass transit, Bus, Airline, ...
'2'	'0' , Y	Financial	IEP, Banking, Retail, ...
'3'	'0' , Y	Identification	Access Control, ...
'4'	'0' , Y	Telecommunication	Public Telephony, GSM, ...
'5'	'0' , Y	Medical	
'6'	'0' , Y	Multimedia	Internet services....
'7'	'0' , Y	Gaming	
'8'	'0' , Y	Data storage	Portable Files, ....
'9' - 'F'	'0' , Y	RFU	

- Remarks: X = '1' to 'F', Y = '1' to 'F'

## (2) Extended Specifications

None

## (3) References

The AFI set for the PICC shall be '00'. The PICC shall not to respond to REQB/WUPB for which AFI is not '00'.

In addition, the PCD shall set AFI = '00' and sends an REQB/WUPB command.

### 12.2.7.4 Coding of PARAM

#### (1) Basic Specifications

Details of encoding of the PARAM byte in the REQB/WUPB commands are shown in "Fig. 12.2-10 Coding of PARAM" and "Table 12.2-2 Encoding of N".

b8 = 0	b7 = 0	b6 = 0	b5 = 0	b4	b3	b2	b1
RFU				REQB / WUPB	N(Number of slots)		

All RFU bits shall be set to 0

Fig. 12.2-10 Coding of PARAM

b4 = 0 defines REQB: PICCs in IDLE State or READY State shall process this command

b4 = 1 defines WUPB: PICCs in IDLE State or READY State or HALT State shall process this command

b1, b2 and b3 are used to code the number of slots N according to "Table 12.2-2 Coding of N".

Table 12.2-2 Coding of N

b3	b2	b1	N
0	0	0	$1 = 2^0$
0	0	1	$2 = 2^1$
0	1	0	$4 = 2^2$
0	1	1	$8 = 2^3$
1	0	0	$16 = 2^4$
1	0	1	RFU
1	1	x	RFU

NOTE: For each PICC, the probability of response (ATQB) in the first slot is  $1/N$ . Thus, if the probabilistic approach is used in the PCD, N is not used to adjust the number of slots but the probability for the PICC to return its ATQB in this unique slot.

(2) Extended Specifications

None

(3) References

The PICC supports time slot type anticollision processing.

The PCD sends a command by setting  $b5 = 1$ .

## 12.2.8 Slot Marker Command (Slot\_MARKER)

### (1) Basic Specifications

After a REQB/WUPB Command, the PCD may send up to (N-1) Slot\_MARKER Commands to define the start of each timeslot.

Slot\_MARKER Commands can be sent:

- after the end of an ATQB message received by the PCD to make the start of the next slot;
- or earlier if no ATQB is received (no need to wait until the end of a slot, if this slot is known to be empty).

It is not mandatory for PICC to support this command. In this case, the PICC shall ignore any Slot\_MARKER Command. The PICC may only send its ATQB after REQB (in the first slot) in a probabilistic approach.

### (2) Extended Specifications

None

### (3) References

The PCD does not send a Slot\_MARKER command.

### 12.2.8.1 Slot Marker Command (Slot\_MARKER) Format

#### (1) Basic Specifications

The slot marker command (Slot\_MARKER) is send out using 3 bytes by the PCD. The format is shown in "Fig. 12.2-11 Slot Marker Command (Slot\_MARKER) Format".

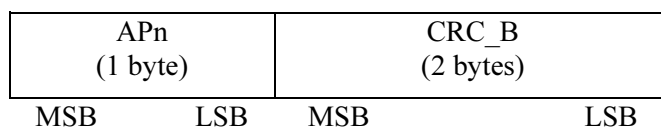


Fig. 12.2-11 Slot Marker Command (Slot\_MARKER) Format

#### (2) Extended Specifications

None

#### (3) References

The PCD does not send a Slot\_MARKER command.



### 12.2.8.2 Coding of Anticollision Prefix byte APn

#### (1) Basic Specifications

The value of the anticollision prefix byte (APn) is  $APn = (nnnn0101)_b$ . Here,  $(nnnn)_b$  is the slot number. The relationship between nnnn and slot number is specified in "Table 12.2-3 Coding of Slot Number".

Table 12.2-3 Coding of Slot Number

Nnnn	Slot nubmer
0001	2
0010	3
0011	4
.....	.....
1110	15
1111	16

NOTE: It is not mandatory that the Slot\_MARKER Commands are sent sequentially with incremental slot numbers.

#### (2) Extended Specifications

None

#### (3) References

The PCD does not send a Slot\_MARKER command.

### 12.2.9 Answer to Request (ATQB)

#### (1) Basic Specifications

The response to both REQB/WUPB and Slot\_MARKER Commands is named ATQB.

#### (2) Extended Specifications

None

#### (3) References

None

### 12.2.9.1 ATQB Format

#### (1) Basic Specifications

The format of ATQB send out from a PICC is shown in "Fig. 12.2-12 ATQB Format".

1st byte	2nd to 5th bytes	6th to 9th bytes	10th to 12th bytes	13th and 14th bytes
'50' (1 byte)	PUPI (4 bytes)	Application data (4 bytes)	Protocol information (3 bytes)	CRC_B (2 bytes)

Fig. 12.2-12 ATQB Format

#### (2) Extended Specifications

None

#### (3) References

None

### 12.2.9.2 Pseudo Unique PICC Identifier (PUPI)

#### (1) Basic Specifications

A Pseudo-Unique PICC Identifier (PUPI) is used to differentiate PICCs during anticollision. This 4-byte number may be either a number dynamically generated by the PICC or a diversified fixed number. The PUPI may only change in the IDLE State.

#### (2) Extended Specifications

None

#### (3) References

None

### 12.2.9.3 Application Data

#### (1) Basic Specifications

The Application data field is used to inform the PCD which applications are currently installed in the PICC. This information allows the PCD to select the desired PICC in the presence of more than one PICC.

The application data is defined dependent upon the ADC (Application Data Coding) field in the Protocol Info, which defines if either the CRC\_B compressing method described below or proprietary coding is used.

When the CRC\_B compressing coding is used, Application Data field contains the following:

1st byte	2nd and 3rd bytes	4th byte
AFI (1 byte)	CRC_B (AID) (2 bytes)	No. of applications (1 byte)

Fig. 12.2-13 Application Data Format

#### (a) AFI

For mono application PICCs AFI gives the family of the application (see Table 12.2-1).

For multi application PICCs AFI gives the family of the application described in CRC\_B (AID).

#### (b) CRC\_B (AID)

CRC\_B (AID) is the result of calculation of CRC\_B of the AID of an application in the PICC matching the AFI given the REQB/WUPB Command.

#### (c) Number of Applications

Indicates on significant half byte value gives the number of application in the PICC.

The most significant half byte value gives the number of applications corresponding to the AFI given in Application Data with '0' meaning no application and 'F' meaning 15 applications or more.

The least significant half byte value gives the total number of applications in the PICC with '0' meaning no application and 'F' meaning 15 application or more.

## (2) Extended Specifications

None

## (3) References

The following values are set for application data.

- 1st to 2nd bytes: Arbitrary value for each IC manufacturer
- 3rd byte: IC manufacturer code specified in ISO/IEC 7816-6 Amendment 1
- 4th byte: 'E0'

### 12.2.9.4 Protocol Info

#### (1) Basic Specifications

The Protocol Info field indicates the parameters supported by the PICC. It is formatted as detailed in "Fig. 12-2-14 Protocol Info Format".

1st byte		2nd byte		3rd byte	
Bit_Rate_capability (8 bits)		Max_Frame_Size (4 bits)	Protpcol_Type (4 bits)	FWI (4 bits)	ADC (2 bits)
MSB	LSB	MSB	LSB	MSB	LSB

Fig. 12-2-14 Protocol Info Format

#### (a) Communication Speed Capability (8 bits)

The capability to support the communication speed of the PICC is shown in "Table 12.2-4 Bit Rates Supported by the PICC".

Table 12.2-4 Bit Rates Supported by the PICC

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
0	0	0	0	0	0	0	0	PICC supports only 106 kbit/s in both directions
1	-	-	-	0	-	-	-	Same bit rate from PCD to PICC and from PICC to PCD compulsory.
-	-	-	1	0	-	-	-	PICC to PCD, 1etu=64 / fc, bit rate supported is 212 kbit/s
-	-	1	-	0	-	-	-	PICC to PCD, 1etu=32 / fc, bit rate supported is 424 kbit/s
-	1	-	-	0	-	-	-	PICC to PCD, 1etu=16 / fc, bit rate supported is 847 kbit/s
-	-	-	-	0	-	-	1	PCD to PICC, 1etu=64 / fc, bit rate supported is 212 kbit/s
-	-	-	-	0	-	1	-	PCD to PICC, 1etu=32 / fc, bit rate supported is 424 kbit/s
-	-	-	-	0	1	-	-	PCD to PICC, 1etu=16 / fc, bit rate supported is 847 kbit/s
Other values (b4 = 1)								PFU

## (b) Maximum Frame Sizes

The maximum frame sizes able to be received by the PICC are shown in "Table 12.2-5 Maximum Frame Sizes".

Table 12.2-5 Maximum Frame Sizes

Maximum Frame Size Code in ATQB	0	1	2	3	4	5	6	7	8	9 - F
Maximum Frame Size(byte)	16	24	32	40	48	64	96	128	256	RFU > 256

## (c) Protocol Type (4 bits)

Protocol types supported by the PICC are defined in "Table 12.2-6 Protocol Types Supported by PICC".

Table 12.2-6 Protocol Types Supported by PICC

b4	b3	b2	b1	Meaning
0	0	0	1	PICC compliant with ISO/IEC 14443-4
0	0	0	0	PICC not compliant with ISO/IEC 14443-4
Other values				RFU

## (d) Frame Waiting Time Integer (FWI) (4 bits)

FWI codes an integer value used to define the frame waiting time (FWT).

The FWT defines the maximum time for a PICC to start its response after the end of a PCD frame.

FWT is calculated by the formula:

$$FWT = (256 \times 16/fc) \times 2^{FWI}$$

where the value of FWI has the range from 0 to 14 and the value of 15 is RFU.

For FWI = 0, FWI is minimal (~ 302 μs)

For FWI = 14, FWI is maximal (~ 4949 ms)



## (e) Application Data Coding (2 bits)

The details of application data coding (ADC) are shown in "Table 12-2-7 Application Data Coding Supported by PICC".

Table 12-2-7 Application Data Coding Supported by PICC

b4	b3	Meaning
0	0	Arbitrary application
0	1	Coding shown in "12.2.9.3 Application Data"
Other values		RFU

## (f) Frame Option (2 bits)

Details of the frame options supported by the PICC are shown in "Table 12-2-8 Frame Options Supported by PICC".

Table 12-2-8 Frame Options Supported by PICC

b2	b1	Meaning
1	x	PICC supports NAD.
x	1	PICC supports CID.

## (2) Extended Specifications

None

## (3) References

The value of application data coding (ADC) shall be (00)b.  
Frame option (FO) shall support CID.

## 12.2.10 ATTRIB Command

### (1) Basic Specifications

The ATTRIB Command sent by the PCD shall include information required to select a single PICC.

A PICC receiving an ATTRIB Command with its identifier becomes selected and assigned to a dedicated channel. After being selected, this PICC only response to commands in ISO/IEC 14443-4 which include its unique CID.

### (2) Extended Specifications

None

### (3) References

None

### 12.2.10.1 ATTRIB Command Format

#### (1) Basic Specifications

ATTRIB Command has the following format: "Fig. 12-2-15 ATTRIB Command format"

'ID'	Identifier	Param1	Param2	Param3	Param4	Higher layer - INF	CRC_B
(1 byte)	(4 byte)	(1 byte)	(1 byte)	(1 byte)	(1 byte)	(Option: 0 byte or more)	(2 byte)

Fig. 12-2-15 ATTRIB Command Format

A CID value of '00' is returned if the PICC does not support CID.

#### (2) Extended Specifications

None

#### (3) References

None

## 12.2.10.2 Identifier

### (1) Basic Specifications

This identifier is the value of the PUPI sent by PICC in the ATQB.

### (2) Extended Specifications

None

### (3) References

None

### 12.2.10.3 Coding of Param 1

#### (1) Basic Specifications

Encoding of PARAM1 within an ATTRIB sent by the PCD is shown in "Fig. 12-2-16 Coding of Param1". All RFU bits shall be set to 0 if not otherwise specified.

Minimum TR0		Minimum TR1		EOF	SOF	RFU	
b8	b7	b6	b5	b4	b3	b2	b1

Fig. 12-2-16 Coding of Param 1

#### (a) EOF/SOF

b3 and b4 indicate the PCD capability to support suppression of the EOF and/or SOF from PICC to PCD, which may reduce communication overhead. The suppression of EOF and/or SOF is optional for the PICC. The coding of b3 and b4 is shown in "Table 12-2-9 Handling of SOF/EOF":

Table 12-2-9 Handling of SOF/EOF

b3	Request to send SOF	b4	Request to send EOF
0	Request	0	Request
1	Not requested (may be omitted)	1	Not requested (may be omitted)

## (b) Minimum TRO

Minimum TRO indicates to the PICC the minimum delay before responding after the end of a command sent by a PCD. The default value has been defined in ISO/IEC 14443-2, 9.2.5..

Encoding of T0 is shown in "Table 12-2-10 Minimum TRO coding".

Table 12-2-10 Minimum TRO coding

b8-b7	Minimum TRO
00	default value
01	48/fs
10	16/fs
11	RFU

NOTE: Minimum TRO is required by the PCD when switching from transmit to receive and its value depends on the PCD performance.

## (c) Minimum TR1

Minimum TR1 indicates to the PICC the minimum delay between subcarrier modulation start and beginning of data transmission. The default value has been defined in ISO/IEC 14443-2, 9.2.5.

Encoding of T1 is shown in "Table 12-2-11 Minimum TR1".

Table 12-2-11 Minimum TR1

b6-b5	Minimum TR1
00	default value
01	64/fs
10	16/fs
11	RFU

NOTE: Minimum TR1 is required by the PCD for synchronization with the PICC and its value depends on the PCD performance.

## (2) Extended Specifications

None

## (3) References

None

## 12.2.10.4 Coding of Param2

### (1) Basic Specifications

The least significant half byte (b4 to b1) is used to code the maximum frame size that can be received by the PCD as specified in "Table 12-2-12 Coding of b4 to b1 of Param2".

Table 12-2-12 Coding of b4 to b1 of Param2

Maximum Frame Size Code in ATTRIB	0	1	2	3	4	5	6	7	8	9-F
Maximum Frame Size(byte)	16	24	32	40	48	64	96	128	256	RFU

NOTE: RFU is retained for the case in which the value is larger than 256.

The most significant half byte (b8 to b5) is used for bit rate selection, as specified in "Table 12-2-13 Coding of b5 to b8 of Param2".

Table 12-2-13 Coding of b5 to b8 of Param2

b6 b5	Meaning
00	PCD to PICC, 1etu = 128 / fc, bit rate is 106 kbit/s
01	PCD to PICC, 1etu = 64 / fc, bit rate is 212 kbit/s
10	PCD to PICC, 1etu = 32 / fc, bit rate is 424 kbit/s
11	PCD to PICC, 1etu = 16 / fc, bit rate is 847 kbit/s

b8 b7	Meaning
00	PICC to PCD, 1etu = 128 / fc, bit rate is 106 kbit/s
01	PICC to PCD, 1etu = 64 / fc, bit rate is 212 kbit/s
10	PICC to PCD, 1etu = 32 / fc, bit rate is 424 kbit/s
11	PICC to PCD, 1etu = 16 / fc, bit rate is 847 kbit/s

### (2) Extended Specifications

None

### (3) References

None

### 12.2.10.5 Coding of Param3

#### (1) Basic Specifications

The least significant half byte (b4 to b1) is used for confirmation of the protocol type as specified in "Table 12.2-6 Protocol Types Supported by PICC". The most significant half byte (b8 to b5) is set to (0000)b, all other value are RFU.

Coding of Param3 is shown in "Table 12-2-17 Coding of Param3 ".

RFU				Protocol type			
b8 = 0	b7 = 0	b6 = 0	b5 = 0	b4	b3	b2	b1

Table 12-2-17 Coding of Param3

#### (2) Extended Specifications

None

#### (3) References

None



## 12.2.10.6 Coding of Param4

### (1) Basic Specifications

The Param 4 byte consists of two parts:

- the least significant half byte (b4 to b1) is named Card Identifier (CID) and defines the logical number of the addressed PICC in the range from 0 to 14. The Value 15 is RFU. The CID is specified by the PCD and shall be unique for each active PICC. If the PICC does not support CID, code value (0000)b shall be used;
- the most significant half byte (b8 to b5) is set to (0000)b, all other values are RFU.

### (2) Extended Specifications

None

### (3) References

None

## 12.2.10.7 Higher layer INF

### (1) Basic Specifications

Any higher layer command transferable as the INF field of ISO/IEC 14443-4 may be included.

It is not mandatory for the PICC to process successfully any command in this context.

The PICC shall however process successfully such message if no application command is included.

### (2) Extended Specifications

None

### (3) References

The following specifications are added to the basic specifications.

Upper layer information: 'F4 XX XX XX XX'

- 1st byte:

Indicates that a matching check is performed on 4 application data bytes (and other values are designated as RFU).

- 2nd to 5th bytes:

Data is the same as application data in ATQB.

If the upper layer information is as described above, when application data in ATQB is identical to the 4 bytes following 'F4' of the upper layer information, a response to ATTRIB is returned and the PICC changes to the ACTIVE state. If they do not match, a response is not returned and the PICC remains in the READY-DECLARED state.

An upper layer response does not exist for the 'F4' command.

Accordingly, a summary of card operation when an ATTRIB command is received for which the PUPI matches is as shown below.

- If upper layer information does not exist, a response is returned and the PICC changes to the ACTIVE state.
- If upper layer information is 'F4 XX XX XX XX' and 'XX XX XX XX' matches with the application data of ATQB, a response is returned and the PICC changes to the ACTIVE state.
- If upper layer information is 'F4 XX XX XX XX' and 'XX XX XX XX' does not match with the application data of ATQB, a response is not returned and the PICC remains in the READY-DECLARED state.

If upper layer information is not 'F4 XX XX XX XX', a response is not returned and the PICC remains in the READY-DECLARED state.

## 12.2.11 Answer to ATTRIB Command

### (1) Basic Specifications

The PICC shall answer to any valid ATTRIB Command (correct PUPI and valid CRC\_B) with the format described in "Fig. 12-2-18 Format of the Answer to an ATTRIB Command".

MBLI (1 byte)	CID	Higher layer Response (Optional 0 or more bytes)	CRC_B (2 bytes)
------------------	-----	---	--------------------

Fig. 12-2-18 Format of the Answer to an ATTRIB Command

The first byte consists of two parts:

- 1) The most significant half byte (b8 to b5) is called the Maximum Buffer Length Index (MBLI). It is used by the PICC to let the PCD know the limit of its internal buffer to received chained frames. The coding of MBLI is as follows:
  - MBLI = 0:
    - means that the PICC provides no information on its internal input buffer size;
  - MBLI > 0:
    - is used to calculate the actual internal maximum buffer length (MBL) according to the following formula:
 
$$MBL = (\text{PICC Maximum Frame Size}) * 2^{(MBLI-1)}$$
 where the PICC maximum frame size is returned accumulated length is never grater than MBL.
- 2) The least significant half byte (b4 to b1) contains the returned CID. If the PICC dose not support CID, code value (0000)b is returned.

As indicated in "Fig. 12-2-19 PICC Answer to ATTRIB Format without Higher Layer Response", a PICC shall the answer the empty (no higher layer INF filed) ATTRIB Command with an empty higher layer response:

MBLI (1 byte)	CID	CRC_B (2 bytes)
------------------	-----	--------------------

Fig. 12-2-19 PICC Answer to ATTRIB Format without Higher Layer Response

NOTE: A suitably formatted ATTRIB response command (for which CID and CRD\_B are set) indicates that the PICC has been selected by the PCD.

## (2) Extended Specifications

None

## (3) References

If the upper layer information satisfies the conditions specified in "12.2.10.7 (3) References", a response is returned in the format specified in "Fig. 12.2-19 PICC Answer to ATTRIB Format without Higher Layer Response".

## 12.2.12 HLTB Command and Answer

### (1) Basic Specifications

The HLTB Command is used to set a PICC in HALT State and stop responding to a REQb. After answering to this command the PICC shall ignore any commands except the WUPB Command (see "12.2.7 REQb/WUPB Command").

The format of a halt command sent out by the PCD is shown in "Fig. 12-2-20 Format of the HLTB Command".

'50' (1 byte)	Identifier (4 bytes)	CRC_B (2 bytes)
------------------	-------------------------	--------------------

Fig. 12-2-20 Format of the HLTB Command

The 4 byte identifier is the value of the PUPI sent by the PICC in the ATQB.

The format of Answer to a HLTB Command from the PICC is shown in "Fig. 12-2-21 Format of PICC Answer to HLTB Command".

'00' (1 byte)	CRC_B (2 bytes)
------------------	--------------------

Fig. 12-2-21 Format of PICC Answer to HLTB Command

### (2) Extended Specifications

None

### (3) References

None

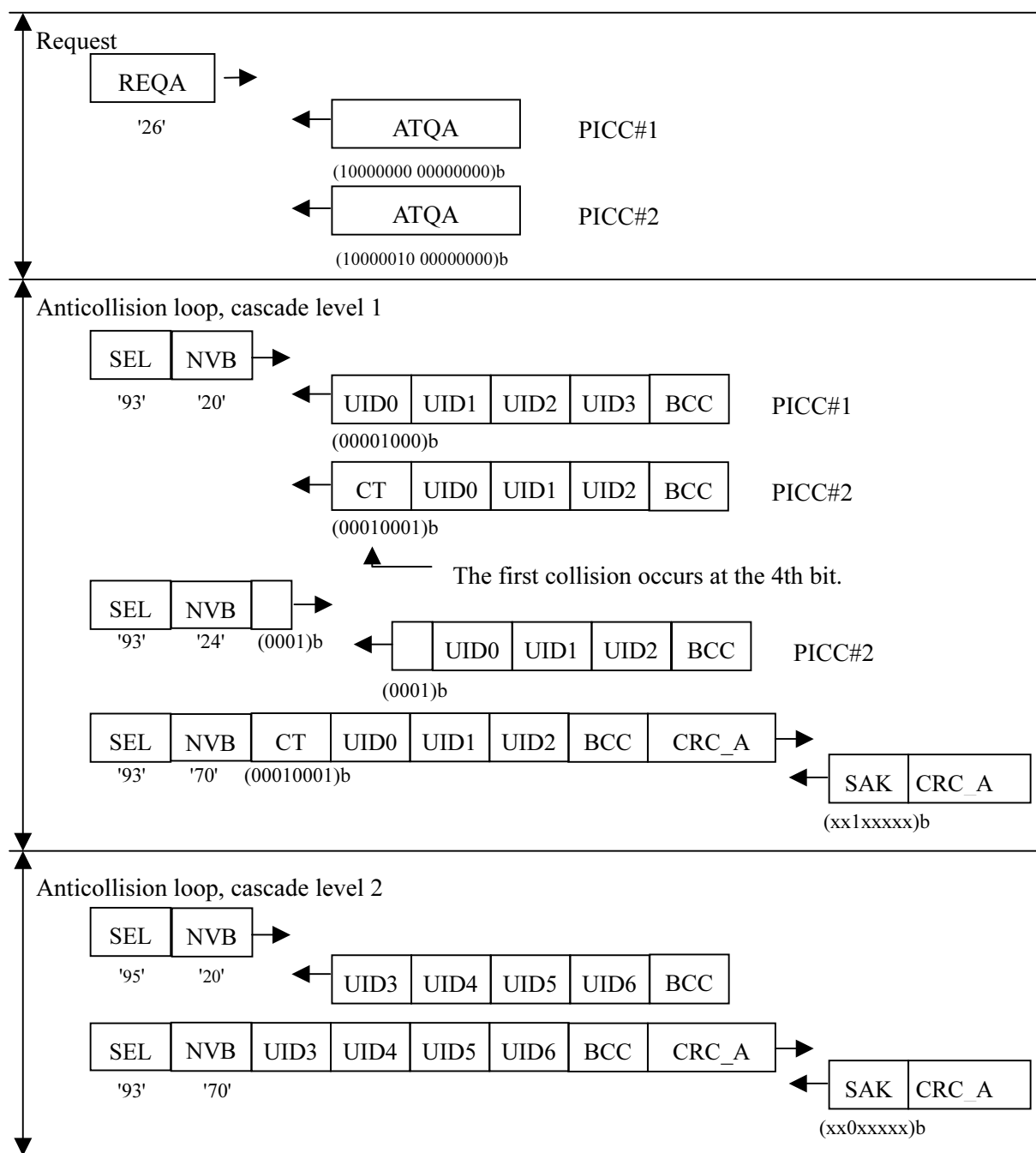
## 12.3 Communication Example Type A

### 12.3.1 Overview of Communication Example of Bit Frame Anticollision Processing

#### (1) Basic Specifications

This example illustrated in "Fig. 12.3-1 Select sequence with bit frame anticollision" shows the select sequence with 2 PICCs in the field on the assumption of:

- PICC #1 with UID size : single, Value of uid0 '10';
- PICC #2 with UID size : double.



Note: start of communication, end of communication and parity bits are not shown for the sake of simplicity.

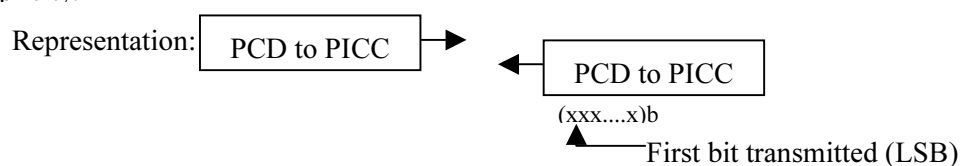


Fig. 12.3-1 Select Sequence with Bit Frame Anticollision

(2) Extended Specifications

None

(3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.



## 12.3.2 Explanation of Selection Processing of Bit Frame Anticollision

### 12.3.2.1 Request Processing

#### (1) Basic Specifications

The contents of the request portion of "Fig. 12.3-1 Select Sequence with Bit Frame Anticollision" are as shown below.

- PCD transmits the REQA Command.
- All PICCs respond with their ATQA.
  - PICC #1 indicates bit frame anticollision and UID size : single.
  - PICC #2 indicates bit frame anticollision and UID size : double.

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.3.2.2 Anticollision Loop, Cascade Level 1

#### (1) Basic Specifications

The contents of the anticollision loop portion of cascade level 1 of "Fig. 12.3-1 Select Sequence with Bit Frame Anticollision" are as shown below.

- PCD transmits an ANTICOLLISION Command:
- SEL specifies bit frame anticollision and cascade level 1;
- the value '20' of NVB specifies that the PCD will transmit no part of UID CL1;
- consequently all PICCs in the field respond with their complete UID CL1;
- due to the value '88' of the cascade tag, the first collection occurs at bit position #4;
- PCD transmits another ANTICOLLISION Command that includes the first 3 bits of UID CL1 that were received before the collision occurs, follow by a (1)b. Consequently the PCD assigns NVB with the value '24';
- these 4bits correspond to the first bits of UID CL1 of PICC #2;
- PICC #2 responds with its 36 remaining bits of UID CL1. Since PICC #1 dose not respond, no collision occurs;
- since the PCD "knows" all bits of UID CL1 of PICC #2, it transmits a SELECT Command for PICC #2;
- PICC #2 responds with SAK, indicating that UID is not complete;
- consequently, the PCD increases the cascade level.

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.3.2.3 Anticollision Loop, Cascade Level 2

#### (1) Basic Specifications

The contents of the anticollision loop portion of cascade level 2 of "Fig. 12.3-1 Select Sequence with Bit Frame Anticollision" are as shown below.

- PCD transmits another ANTICOLLISION Command:
  - SEL specifies bit frame anticollision and cascade level 2;
  - NVB is reset to '20' to force PICC #2 to respond with its complete UID CL2;
- PICC #2 responds with all 40 bits of its UID CL2;
- PCD transmits the SELECT Command for PICC #2, cascade level 2;
- PICC #2 responds with SAK indicating that the UID is complete, and switches from the READY state to the ACTIVE state.

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

## 12.4 CRC\_A and CRC\_B Encoding

### 12.4.1 CRC\_A Encoding

#### (1) Basic Specifications

This section is provided for explanatory purposes and indicates the bit patterns that will exist in the physical layer. It is included for the purpose of checking an ISO/IEC 14443-3 Type A implementation of CRC\_A encoding.

The process of encoding and decoding may be conveniently carried out by a 16-stage cyclic shift register with appropriate feedback gates. According to ITU-T Recommendation V.41, ANNEX I, figures I-1/V.41, and 1-2/V.41 the flip-flops of the register shall be numbered from FFO to FF15. FFO shall be the leftmost flip-flop where data is shifted in. FF15 shall be the rightmost flip-flop where data is shifted out..

The initial value of the register is shown in "Table 12.4-1 Initial Content of 16-Stage Shift Register According to Value '6363'".

Table 12.4-1 Initial Content of 16-Stage Shift Register According to Value '6363'

FF0	FF1	FF2	FF3	FF4	FF5	FF6	FF7	FF8	FF9	FF10	FF11	FF12	FF13	FF14	FF15
0	1	1	0	0	0	1	1	0	1	1	0	0	0	1	1

The initial value is set to '6363' in hexadecimal. Consequently, FFO corresponds to the MSB and FF15 to the LSB.

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.4.1.1 CRC\_A Example 1

#### (1) Basic Specifications

The following conditions are used for CRC\_A example 1.

- Transmission of data, first byte = '00', second byte = '00', CRC\_A appended.

According to the calculation result of this example, CRC\_A = '1EA0'. The frame organization in this case is shown in "Fig. 12.4-1 Example 1 for CRC\_A Encoding". In addition, the final contents of the shift register during encoding are shown in "Table 12.4-2 Content of 16-stage Shift Register According to Value '1EA0'".

First bit transmitted

↓

S	0000 0000	1	0000 0000	1	0000 0101	1	0111 1000	1	E
	'00'	P	'00'	P	'A0'	P	'1E'	P	

Fig. 12.4-1 Example 1 for CRC\_A Encoding

Table 12.4-2 Content of 16-stage Shift Register According to Value '1EA0'

FF0	FF1	FF2	FF3	FF4	FF5	FF6	FF7	FF8	FF9	FF10	FF11	FF12	FF13	FF14	FF15
0	0	0	1	1	1	1	0	1	0	1	0	0	0	0	0

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

### 12.4.1.2 CRC\_A Example 2

#### (1) Basic Specifications

The following conditions are used for CRC\_A example 2.

- Transmission of data block, first byte = '12', second byte = '34', CRC\_A appended.

According to the calculation result of this example, CRC\_A = 'CF26'. The frame organization in this case is shown in "Fig. 12.4-2 Example 2 for CRC\_A encoding". In addition, the final contents of the shift register during encoding are shown in "Table 12.4-3 Content of 16-stage shift register according to value 'CF26'".

First bit transmitted

↓

S	0100 1000	1	0010 1100	0	0110 0100	0	1111 0011	1	E
	'12'	P	'34'	P	'26'	P	'CF'	P	

Fig. 12.4-2 Example 2 for CRC\_A Encoding

Table 12.4-3 Content of 16-stage Shift Register According to Value 'CF26'

FF0	FF1	FF2	FF3	FF4	FF5	FF6	FF7	FF8	FF9	FF10	FF11	FF12	FF13	FF14	FF15
1	1	0	0	1	1	1	1	0	0	1	0	0	1	1	0

#### (2) Extended Specifications

None

#### (3) References

"12.5 Type A Timeslot - Initialization and Anticollision" is employed.

## 12.4.2 CRC\_B Encoding

### (1) Basic Specifications

This section is provided for explanatory purpose and indicates the bit patterns that will exist in the physical layer. It is included for the purpose of checking an ISO/IEC 14443-3 Type B implementation of CRC\_B encoding.

Refer to ISO/IEC 13239 and CCITT X.25 #2.2.7 and V.42 #8.1.1.6.1 for further details.

Initial Value = 'FFFF'

### (2) Extended Specifications

None

### (3) References

None

### 12.4.2.1 CRC\_B Example 1

#### (1) Basic Specifications

The following conditions are used for CRC\_B example 1.

- Transmission of first byte = '00', second byte = '00', third byte = '00', CRC\_B appended.

According to the calculation result of this example, CRC\_B = 'C6CC'. The frame organization in this case is shown in "Fig. 12.4-3 Example 1 for CRC\_B encoding".

	1st byte	2nd byte	3rd byte	CRC_B		
SOF	'00'	'00'	'00'	'CC'	'C6'	EOF

Fig. 12.4-3 Example 1 for CRC\_B encoding

#### (2) Extended Specifications

None

#### (3) References

None



### 12.4.2.2 CRC\_B Example 1

#### (1) Basic Specifications

The following conditions are used for CRC\_B example 2.

- Transmission of first byte = '0F', second byte = 'AA', third byte = 'FF', CRC\_B appended.

According to the calculation result of this example, CRC\_B = 'D1FC'. The frame organization in this case is shown in "Fig. 12.4-4 Example 2 for CRC\_B Encoding".

	1st byte	2nd byte	3rd byte	CRC_B		
SOF	'0F'	'AA'	'FF'	'FC'	'D1'	EOF

Fig. 12.4-4 Example 2 for CRC\_B Encoding

#### (2) Extended Specifications

None

#### (3) References

None

### 12.4.2.3 CRC\_B Example 3

#### (1) Basic Specifications

The following conditions are used for CRC\_B example 3.

- Transmission of first byte = '0A', second byte = '12', third byte = '34', fourth byte = '56', CRC\_B appended.

According to the calculation result of this example, CRC\_B = 'F62C'. The frame organization in this case is shown in "Fig. 12.4-5 Example 3 for CRC\_B Encoding".

	1st byte	2nd byte	3rd byte	4th byte	2nd byte		3rd byte
SOF	'0A'	'12'	'34'	'56'	'2C'	'F6'	EOF

Fig. 12.4-5 Example 3 for CRC\_B Encoding

#### (2) Extended Specifications

None

#### (3) References

None

### 12.4.3 Code Sample Written in C Language for CRC Calculation

#### (1) Basic Specifications

```

#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <ctype.h>
#define CRC_A 1
#define CRC_B 2
#define BYTE unsigned char

unsigned short UpdateCrc(unsigned char ch, unsigned short *lpwCrc)
{
    ch = (ch^(unsigned char)((*lpwCrc) & 0x00FF));
    ch = (ch^(ch<<4));

    *lpwCrc = (*lpwCrc >> 8)^((unsigned short)ch << 8)^((unsigned short)ch<<3)^((unsigned
short)ch>>4);

    return(*lpwCrc);
}

void ComputeCrc(int CRCType, char *Data, int Length,
    BYTE *TransmitFirst, BYTE *TransmitSecond)
{
    unsigned char chBlock;
    unsigned short wCrc;

    switch(CRCType) {
        case CRC_A:
            wCrc = 0x6363;    // ITU-V.41
            break;
        case CRC_B:
            wCrc = 0xFFFF;    // ISO 13239
            break;
        default:

```

```

        return;
    }

    do {
        chBlock = *Data++;
        UpdateCrc(chBlock, &wCrc);
    } while (--Length);
    if (CRCType == CRC_B)
        wCrc = ~wCrc;    // ISO 13239

    *TransmitFirst = (BYTE) (wCrc & 0xFF);
    *TransmitSecond = (BYTE) ((wCrc >> 8) & 0xFF);

    return;
}

BYTE BuffCRC_A[10] = {0x12, 0x34};
BYTE BuffCRC_B[10] = {0x0A, 0x12, 0x34, 0x56};
unsigned short Crc;
BYTE First, Second;
FILE *OutFd;
int i;

int main(void)
{
    printf("CRC-16 reference results 3-Jun-1999\n");
    printf("by Mickey Cohen - mickey@softchip.com\n\n");
    printf("Crc-16 G(x) = x^16 + x^12 + x^5 + 1\n\n");

    printf("CRC_A of [ ");
    for(i=0; i<2; i++) printf("%02X ", BuffCRC_A[i]);
    ComputeCrc(CRC_A, BuffCRC_A, 2, &First, &Second);
    printf("] Transmitted: %02X then %02X.\n", First, Second);

    printf("CRC_B of [ ");
    for(i=0; i<4; i++) printf("%02X ", BuffCRC_B[i]);
    ComputeCrc(CRC_B, BuffCRC_B, 4, &First, &Second);
    printf("] Transmitted: %02X then %02X.\n", First, Second);

```

```
    return(0);  
}
```

(2) Extended Specifications

None

(3) References

None

## 12.5 Type A Timeslot - Initialization and Anticollision

This section specifies initialization and anticollision processing for the type A timeslot type PICCs.

The symbols used in this section are indicated below.

- ATH\_t      Answer To Halt of type A\_timeslot
- ATQA\_t     Answer To reQuest of Type A\_timeslot
- ATQ-ID     Answer To REQ-ID
- CID\_t      Card Identifier of Type A\_timeslot
- HLTA\_t     HALT Command of Type A\_timeslot
- REQA\_t     REQuest Command of Type A\_timeslot
- REQ-ID     REQuest-ID Command
- SAK\_t      Select AKnowledge of Type A\_timeslot
- SEL\_t      SElect Command of Type A\_timeslot

## 12.5.1 Bit, Byte and Frame Format

### 12.5.1.1 Timing Definitions

#### (1) Basic Specifications

##### (a) Polling reset time

Polling reset times of Type A\_timeslot are equal to those of Type A in "11. Polling".

##### (b) Time interval from REQA\_t to ATQA\_t

PICC returns ATQA\_t after waiting for  $32 \pm 2$  etu upon receiving REQA\_t. The PCD may not recognize the coding of the ATQA\_t.

##### (c) Request Guard Time

The Request Guard Time is defined as the minimum time between the start of bits of two consecutive Request commands. Its values shall be 0.5 ms.

##### (d) Frame Guard Time

The Fame Guard Time is defined as the minimum time between the rising edge of the last bit and the falling edge of the start bit of two consecutive frames in opposite direction. Its value shall be 10 etu.

##### (e) Timeslot length

The first timeslot starts in 32 etu after REQ-ID. Each timeslot length is 104 etu consisting of 94 etu for ATQ-ID reception and 10 etu frame guard time succeeding.

#### (2) Extended Specifications

None

#### (3) References

None

### 12.5.1.2 Frame Format

#### (1) Basic Specifications

##### (a) REQA\_t Frames

Refer to "12.1.1.5(1)(a) Short Frame" and "Table 12.1-2 Short Frame" for information on the frame format of REQA\_t. The data content is '35' for a REQA\_t.

##### (b) Standard Frames

The LSB of each byte is transmitted first. Each byte has no parity. CRC\_B defined in "12.2.2 Cyclic Redundancy Check Code (CRC\_B)" is added to the end of the frame data. The format of standard frames is shown in "Fig. 12.5-1 Standard Frames of Type A Timeslot Type".

S	1 byte Command/response	Data: $n \times (8 \text{ data bits} + \text{no parity})$			CRC_B 2 bytes	E
		(0 or 1 byte) (Parameter 1)	(0 or 1 byte) (Parameter 2)	(0 or 8 bytes) (UID)		

Fig. 12.5-1 Standard Frames of Type A Timeslot Type

#### (2) Extended Specifications

None

#### (3) References

None



## 12.5.2 PICC States

The following sections provide the states for PICC, Type A\_timeslot.

### 12.5.2.1 Power Off State

#### (1) Basic Specifications

In the POWER-OFF State, the PICC is not energized due to lack of carrier and shall not emit subcarrier.

#### (2) Extended Specifications

None

#### (3) References

None

### 12.5.2.2 IDLE State

#### (1) Basic Specifications

This state is entered after the field has been active within a 5 ms delay. The PICC recognize REQA\_t.

#### (2) Extended Specifications

None

#### (3) References

None

### 12.5.2.3 READY State

#### (1) Basic Specifications

This state is entered by REQA\_t. The PICC recognizes REQA\_t, REQ-ID and SEL\_t.

#### (2) Extended Specifications

None

#### (3) References

None

#### 12.5.2.4 ACTIVE State

##### (1) Basic Specifications

This state has two substates.

The first sub-state is entered by SEL\_t with its complete UID and CID\_t. In this sub-state, the PICC recognizes HLTA\_t and proprietary higher layer commands.

The second sub-state is a state where commands defined in "13.3 Half-duplex Block Transmission Protocol" can be executed, and is entered from the first sub-state by a command defined in "13.1 Protocol Activation of PICC Type A".

##### (2) Extended Specifications

None

##### (3) References

None

### 12.5.2.5 HALT State

#### (1) Basic Specifications

This state is entered by HLTA\_t from ACTIVE State. In this state, the PICC is mute.

#### (2) Extended Specifications

None

#### (3) References

None

### 12.5.3 Command/Response Sets

#### (1) Basic Specifications

Four commands and their response are used. Details are shown in "Table 12.5-1 Commands/Responses of Type A Timeslot Type".

Table 12.5-1 Commands/Responses of Type A Timeslot Type

Type	Name	Encoding (b8-b1)	Meaning
Command	REQA_t	(b7-b1) (0110101)b(='35')	Request PICC Type A timeslot to answer ATQA_t.
Response	ATQA_t	Any value from '00' to 'FF'	Answer to REQA_t. PCD can recognize the existence of Type A timeslot PICC. However, the PCD is not required to recognize the coding of the ATQA_t.
Command	REQ-ID	(00001000)b(='08') Refer to "Table 12.5-2 Parameters of REQ-ID Command" for information on the parameters.	Request the PICC to answer its UID to one to timeslots. REQ-ID is followed by two parameters.
Response	ATQ-ID	(00000110)b(='06')	Answer 8-byte UID to one of 4 timeslots. ATQ-ID is followed by its 8-byte UID.
Command	SEL_t	(01000NNN)b: NNN is CID_t from 0 to 7 (01100NNN)b: NNN+8 is CID_t from 8 to 15	Select the PICC with its UID and set the CID_t. SEL_t is followed by 8 byte UID.
Response	SAK_t	b8-b5(1000)b: Able to acquire additional information with upper layer protocol b8-b5(1100)b: Initial value of protocol b4-b1(0000)b: Other than ISO/IEC 14443-4 b4-b1(0001)b: ISO/IEC14443-4	Acknowledgment of SEL_t
Command	HLTA_t	(00011NNN)b: NNN is CID_t from 0 to 7 (00111NNN)b: NNN+8 is CID_t from 8 to 15	Halt command for PICC of CID_t
Response	ATH_t	(00000110)b(='06')	Acknowledgment of HLTA_t

Coding of parameters in the REQ-ID command is shown in "Table 12.5-2 Parameters of REQ-ID Command".

Table 12.5-2 Parameters of REQ-ID Command

Parameter		Meaning
P1	b8 -b7	Timeslot length, b7=1: for 8-byte UID, b8=0
	b6 - b1	Number of timeslots, b3=1: for 4 timeslots, Others=0
P2		'00'

(2) Extended Specifications

None

(3) References

None



#### 12.5.4 Time Slot Type Anticollision Processing

##### (1) Basic Specifications

The flow chart of PICC anticollision sequence is shown as below in "Fig. 12.5-2 Flowchart of PICC Anticollision Sequence".

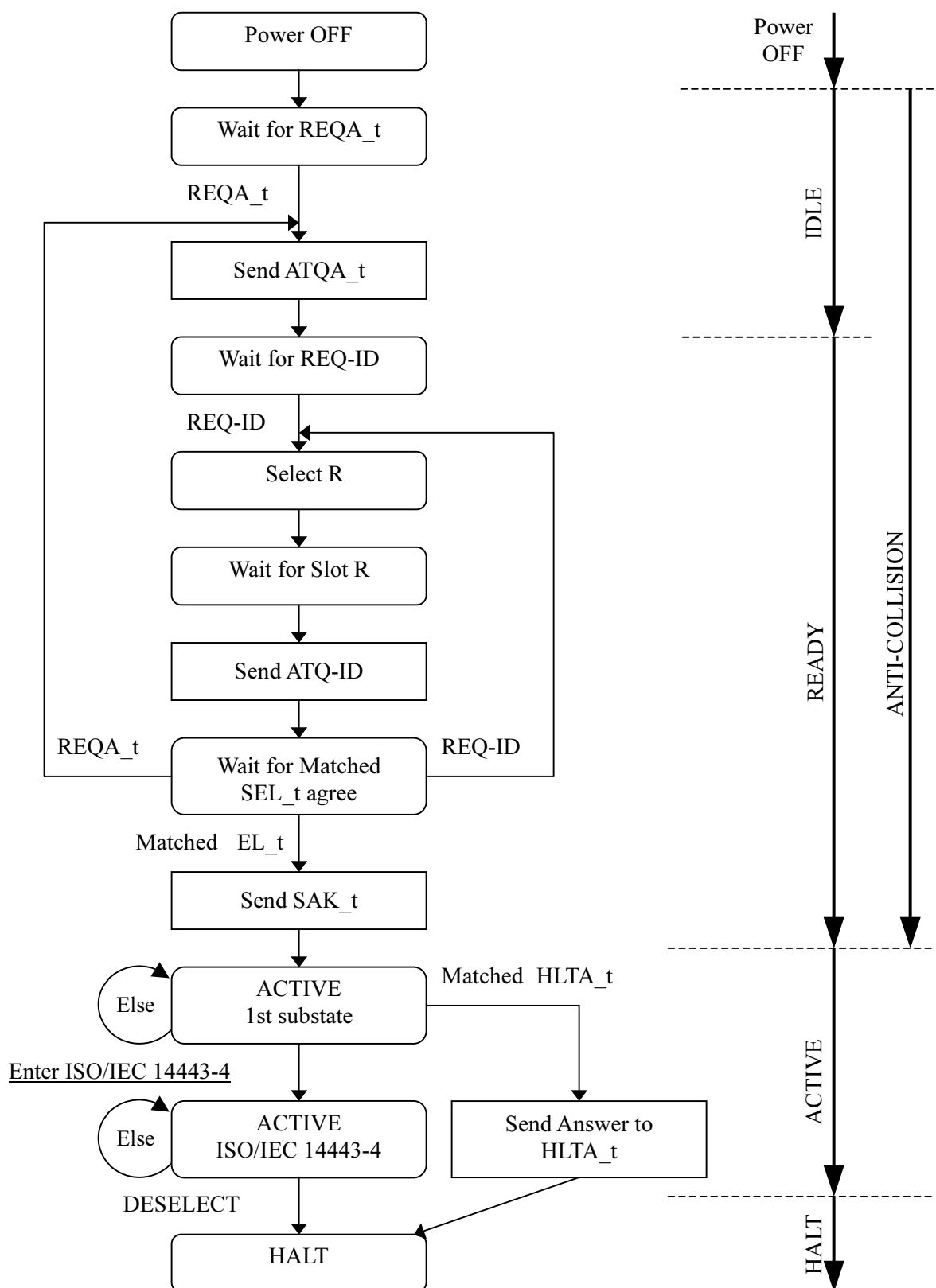


Fig. 12.5-2 FlowChart of PICC Anticollision Sequence

(2) Extended Specifications

None

(3) References

None

## 12.6 Example of Anticollision Sequence for Type B

### (1) Basic Specifications

An example of an anticollision sequence for Type B is shown in "Fig. 12.6-1 Type B Anticollision Sequence Example".

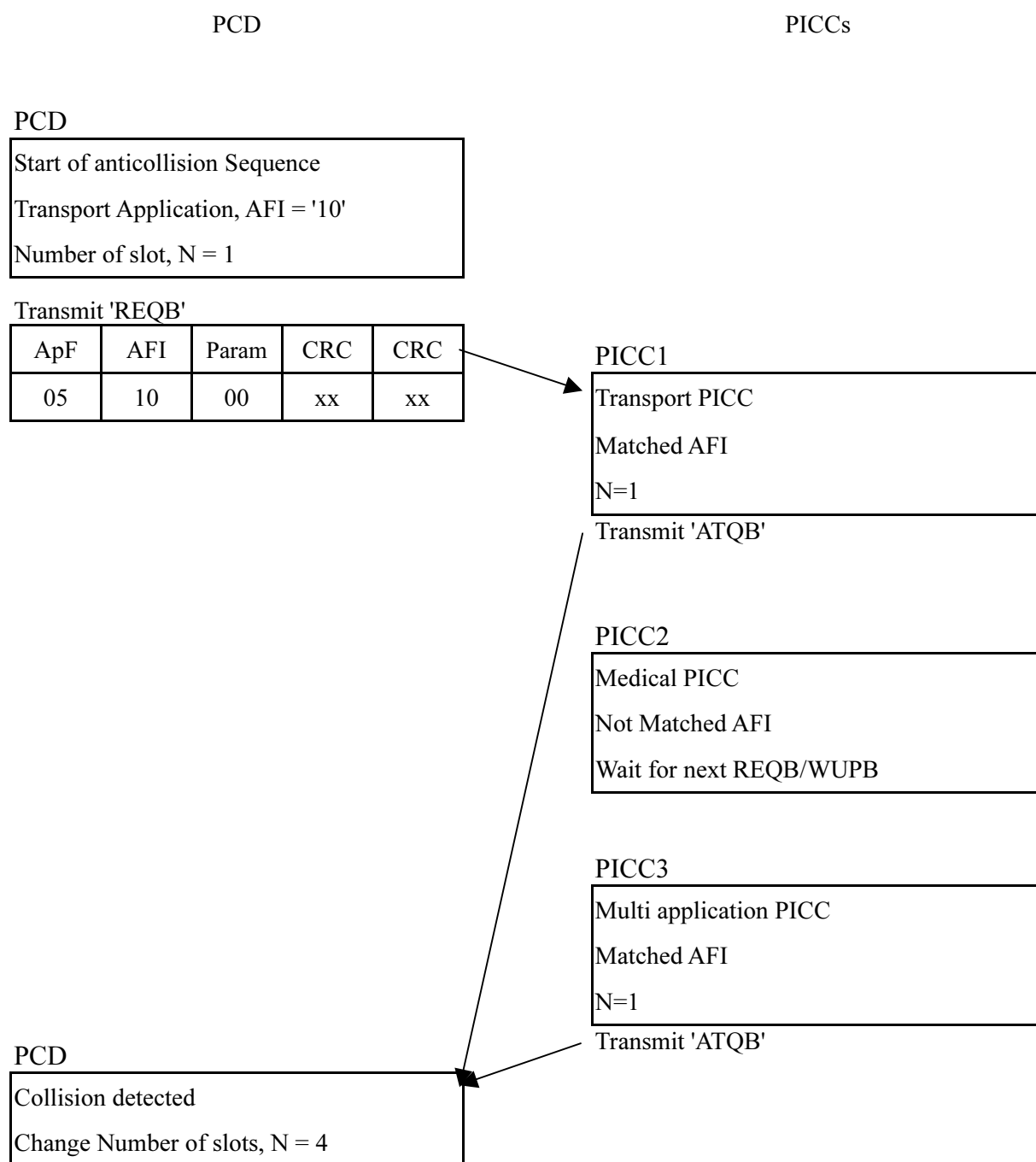


Fig. 12.6-1 Type B Anticollision Sequence Example

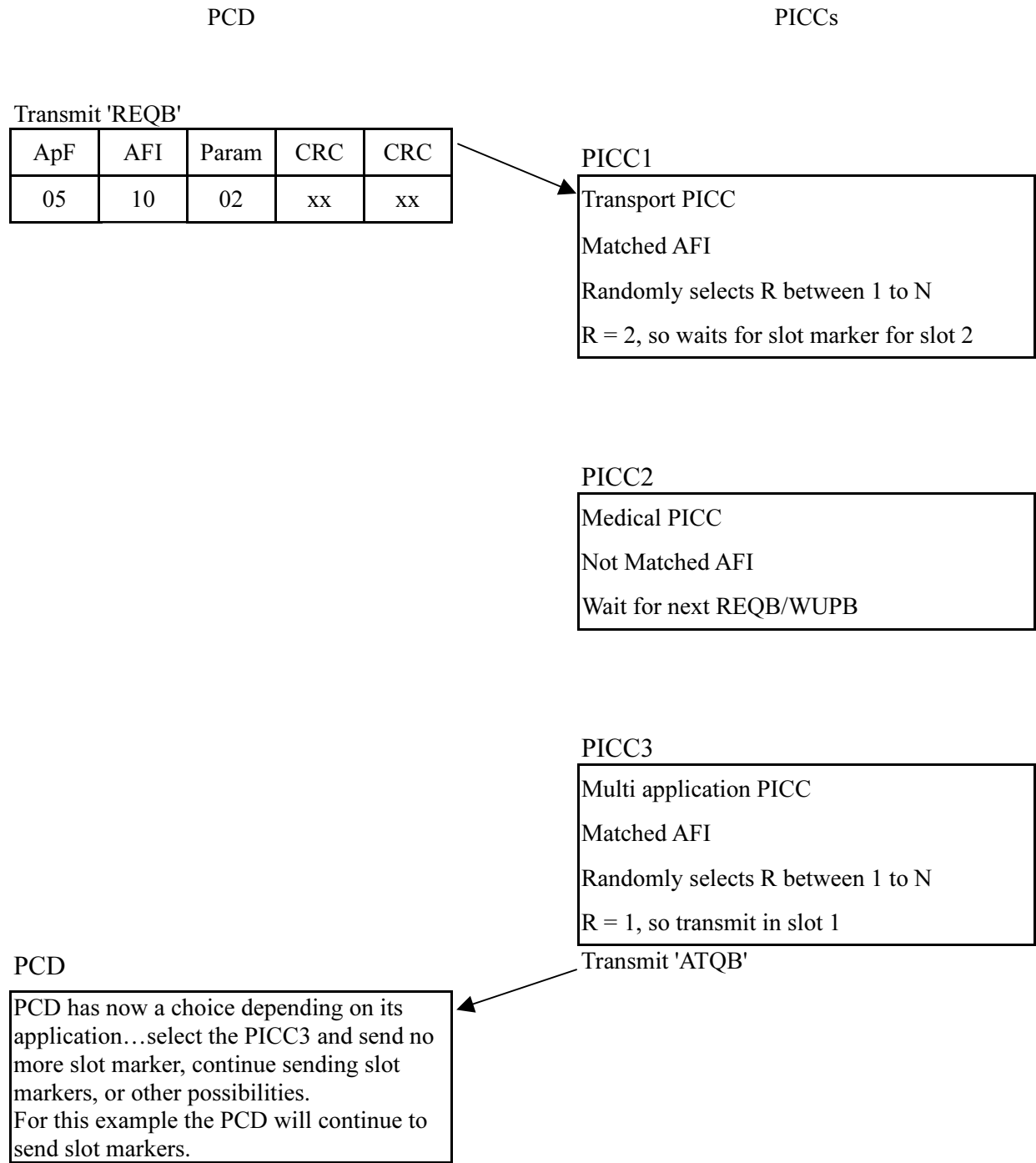


Fig. 12.6-1 Type B Anticollision Sequence Example (continued)

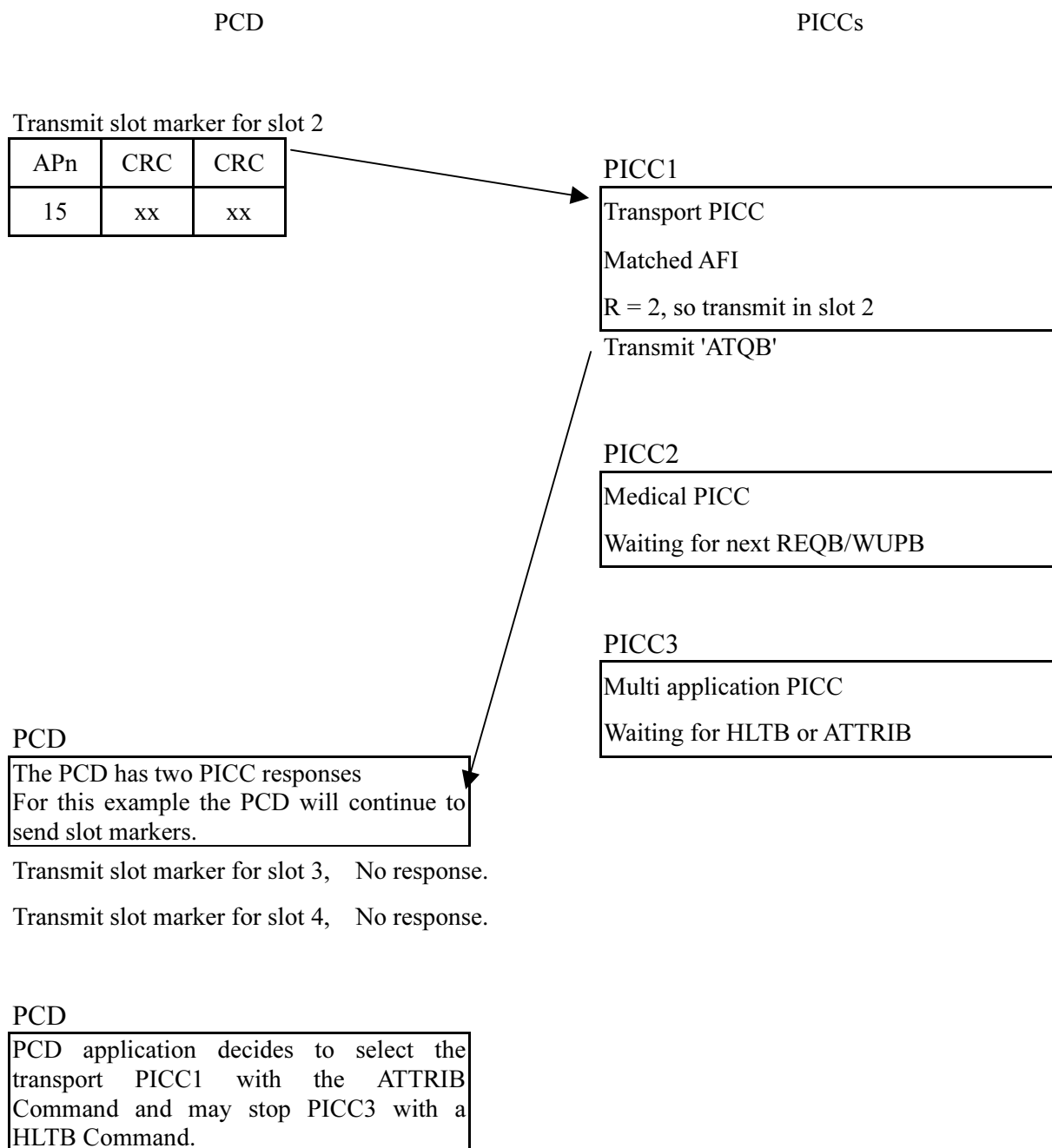


Fig. 12.6-1 Type B Anticollision Sequence Example (continued)

(2) Extended Specifications

None

(3) References

An example of the procedure in the case b5 of the PARAM portion of REQB/WUPB is 1 is shown in "Fig. 12.6-2 Type B Anticollision Sequence Example".

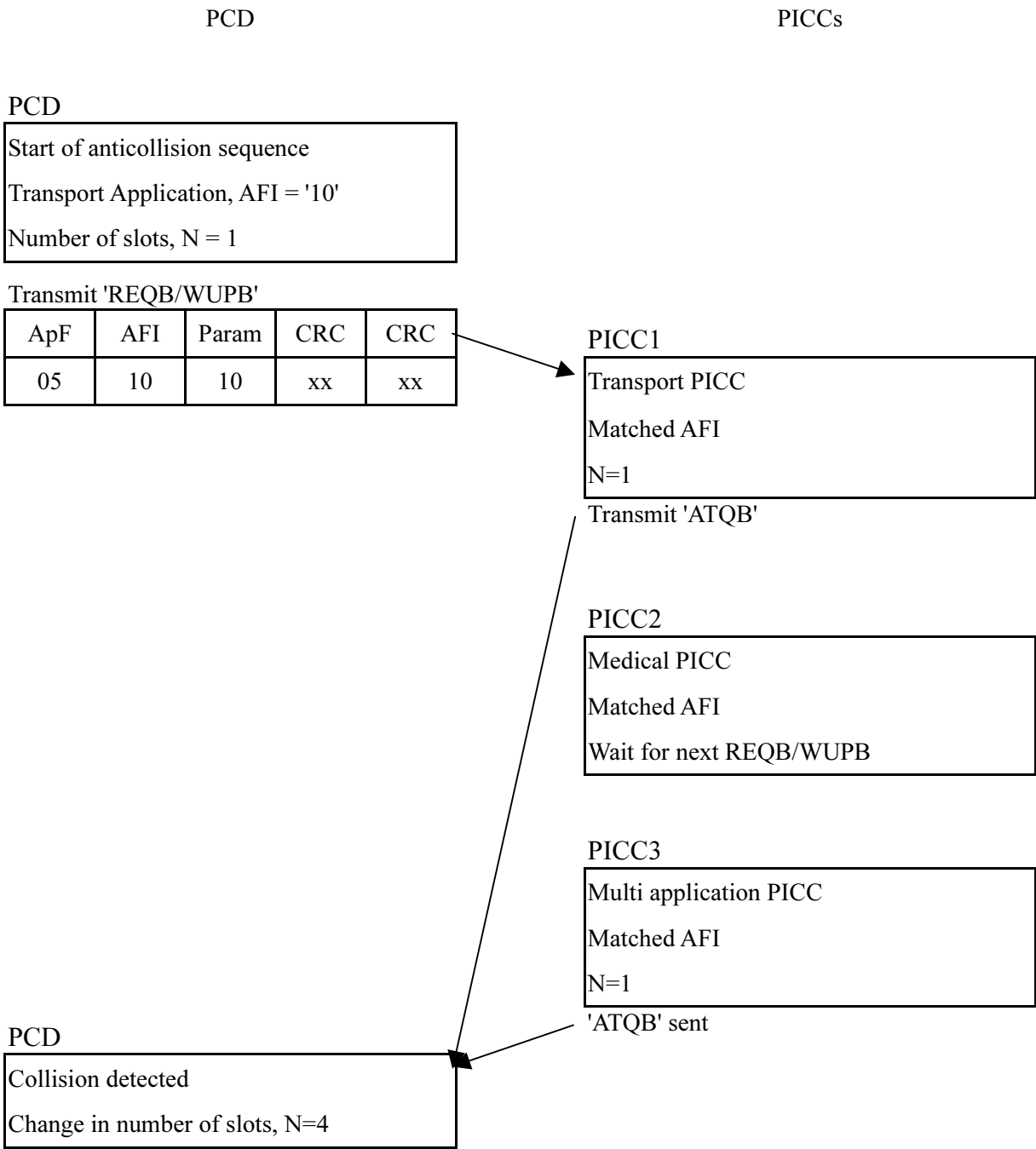


Fig. 12.6-2 Type B Anticollision Sequence Example

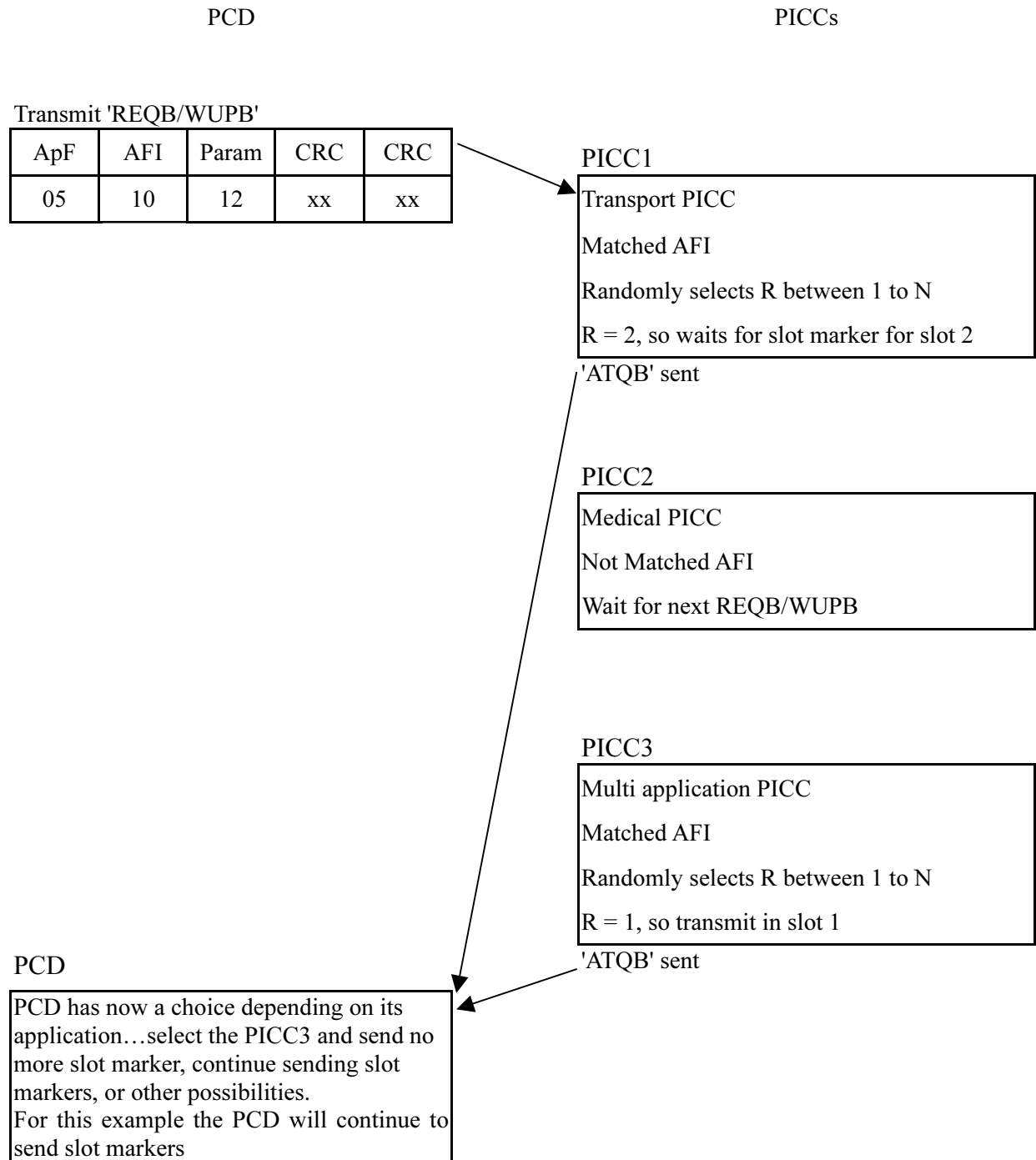


Fig. 12.6-2 Type B Anticollision Sequence Example (continued)



## 13. Transmission Protocol

Communication frames and the basic communication sequence are specified with the transmission protocol of the PICC and PCD on the basis of ISO/IEC 14443-4. Type A and Type B communication formats are specified.

### (1) Terms Used in this Chapter

- Bit duration  
one elementary time unit (etu), calculated by the following formula.
- $1 \text{ etu} = 128 / (D \times f_c)$   
Since the initial value of divisor D is 1, the initial value of etu is as shown below.
- $1 \text{ etu} = 128 f/c$   
fc is specified in "8. Power Transfer".
- Block  
special type of frame, which contains a valid protocol data format. A valid protocol data format includes I-Blocks, R-Blocks or S-Blocks.
- Invalid block  
A type of frame with an invalid protocol format. A time-out, when no frame has been received, is not interpreted as an invalid block.
- Frame  
sequence of bits as defined in "12. Anticollision". The PICC Type A uses the standard frame defined for Type A and the PICC Type B uses the frame defined for Type B.

## (2) Symbols and Abbreviations Used in this Chapter

- ACK positive ACKnowledgement
- ATS Answer To Select
- ATQB Answer To reQuest, Type B
- CID Card IDentifier
- CRC Cyclic Redundancy Check, as defined for each PICC Type in ISO/IEC 14443-3
- D Divisor
- DR Divisor Receive (PCD to PICC)
- DRI Divisor Receive Integer (PCD to PICC)
- DS Divisor Send (PICC to PCD)
- DSI Divisor Send Integer (PICC to PCD)
- EDC Error Detection Code
- etu elementary time unit
- fc carrier frequency
- FSC Frame Size for proximity Card
- FSCI Frame Size for proximity Card Integer
- FSD Frame Size for proximity coupling Device
- FSDI Frame Size for proximity coupling Device Integer
- FWI Frame Waiting time Integer
- FWT Frame Waiting Time
- FWT<sub>TEMP</sub> temporary Frame Waiting Time
- HLTA HALT Command, Type A
- I-Block Information block
- INF INformation Field
- NAD Node ADdress
- OSI Open Systems Interconnection
- PCB Protocol Control Byte
- PCD Proximity Coupling Device
- PICC Proximity Card
- PPS Protocol and Parameter Selection

- PPSS protocol and Parameter Selection Start
- PPS0 Protocol and Parameter Selection parameter 0
- PPS1 Protocol and Parameter Selection parameter 1
- R-Block Receive ready block
- R(ACK) R-Block containing a positive acknowledge
- R(NAK) R-Block containing a negative acknowledge
- RATS Request for Answer To Select
- RFU Reserved for Future Use
- S-Block Supervisory block
- SAK Select AcKnowledge
- SFGI Start-up Frame Guard time Integer
- SFGT Start-up Frame Guard Time
- WUPA Wake-Up Command, Type A
- WTX Waiting Time eXtension
- WTXM Waiting Time eXtension Multiplier

(3) Methods Used to Represent Data Values Used in this Chapter

- (xx)b: Binary xx
- 'xx': Hexadecimal xx

## 13.1 Protocol Activation of PICC Type A

### (1) Basic Specifications

The following activation sequence shall be applied:

- PICC activation sequence as defined in "12. Anticollision" (request, anticollision loop and select).
- At the beginning the SAK byte shall be checked for availability of an ATS. The SAK is defined in "12. Anticollision".
- The PICC may be set to HALT state, using the HLTA Command as defined in "12. Anticollision", if no ATS is available.
- The RATS may be sent by the PCD as next command after receiving the SAK if an ATS is available.
- The PICC shall send its ATS as answer to the RATS. The PICC shall only answer to the RATS if the RATS is received directly after the selection.
- If the PICC supports any changeable parameters in the ATS, a PPS request may be used by the PCD as the next command after receiving the ATS to change parameters.
- The PICC shall send a PPS Response as answer to the PPS request.  
A PICC does not need to implement the PPS, if it does not support any changeable parameters in the ATS.

The PCD activation sequence for a PICC Type A is shown in "Fig. 13.1-1 Activation of a PICC Type A by a PCD".

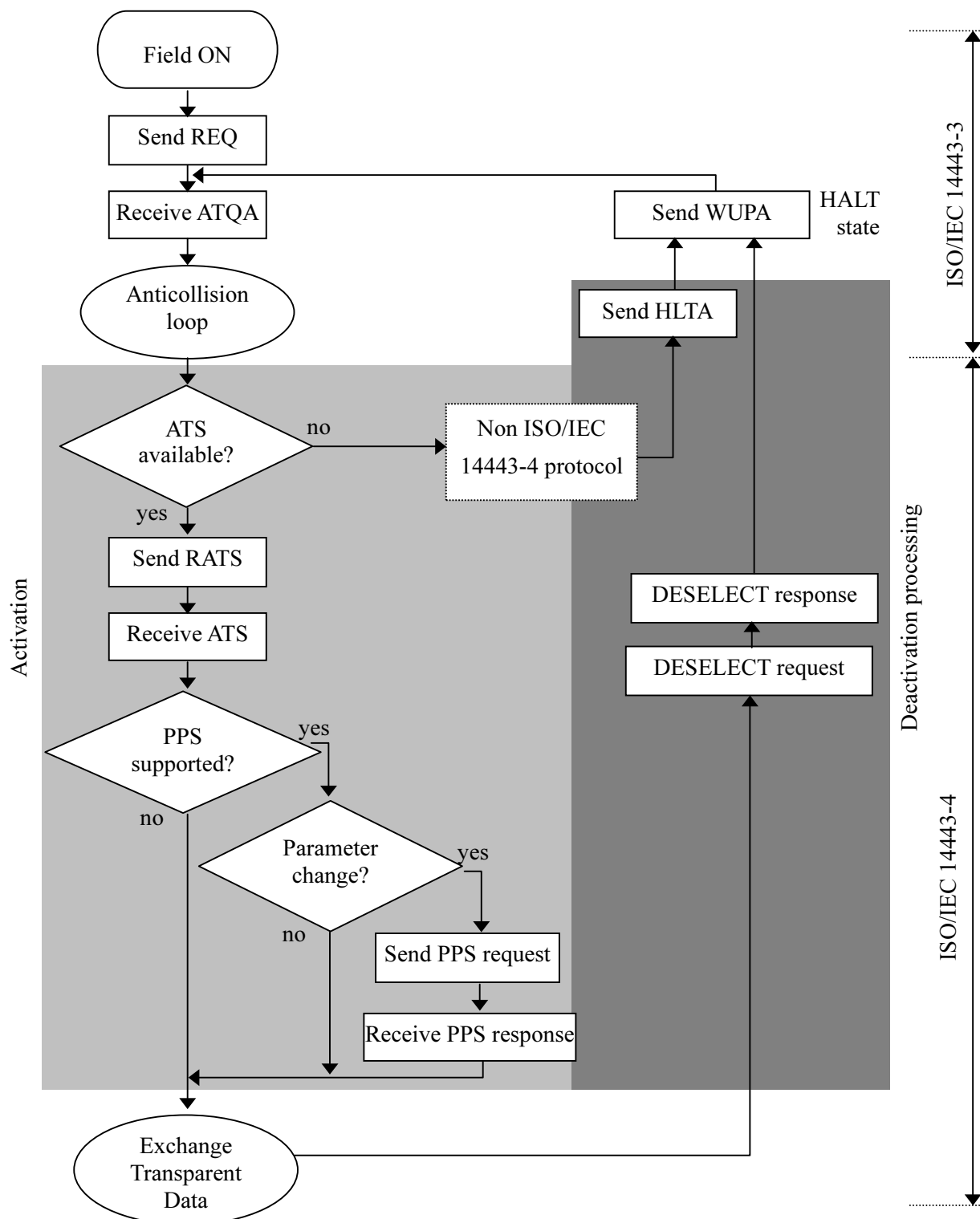


Fig. 13.1-1 Activation of a PICC Type A by a PCD

(2) Extended Specifications

None

(3) References

None

### 13.1.1 Request for Answer to Select

#### (1) Basic Specifications

The specifications of request for ATS (RATS) and its contents are as follows. The structure of RATS is shown in "Fig. 13.1-2 Request for answer to select".

'E0'	Parameter	CRC
1 byte	1 byte	2 bytes

Fig. 13.1-2 Request for answer to select

The parameter byte consists of two parts as shown in "Fig. 13.1-3 Coding of RATS parameter byte".

- The most significant half-byte b8 to b5 is called FSDI and codes FSD. The FSD defines the maximum size of a frame the PCD is able to receive. The coding of FSD is given in "Table 13.1-1 FSDI to FSD conversion".

The least significant half byte b4 to b1 is named CID and it defines the logical number of the addressed PICC in the range from 0 to 14. The value 15 is RFU. The CID is specified by the PCD and shall be unique for all PICCs, which are in the range from 0 to 14. The value 15 is RFU. The CID is specified by the PCD and shall be unique for all PICCs, which are in the ACTIVE state at the same time. The CID is fixed for the time the PICC is active and the PICC shall use the CID as its logical identifier, which is contained in the first error-free RATS received.

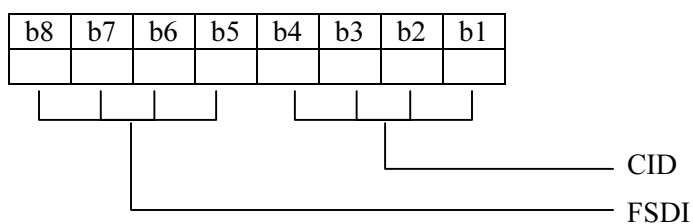


Fig. 13.1-3 Coding of RATS Parameter Byte

Table 13.1-1 FSDI to FSD Conversion

FSDI	'0'	'1'	'2'	'3'	'4'	'5'	'6'	'7'	'8'	'9' to 'F'
FSD	16	24	32	40	48	64	96	128	256	RFU

(2) Extended Specifications

None

(3) References

None



### 13.1.2 Answer to Select (ATS)

#### (1) Basic Specifications

This clause defines the ATS with all its available fields "Fig. 13.1-4 Structure of the ATS".

In the case that one of the defined fields is not present in an ATS sent by a PICC the default values for that field shall apply.

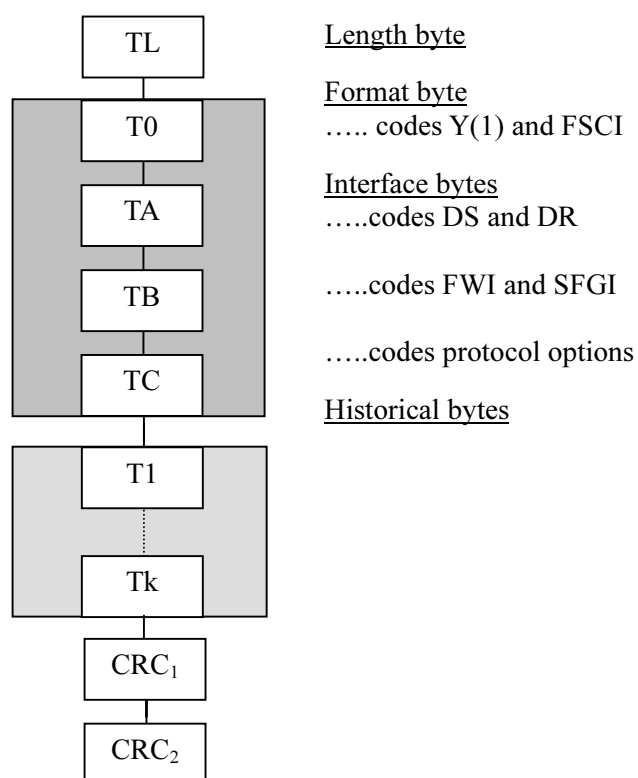


Fig. 13.1-4 Structure of the ATS

#### (2) Extended Specifications

None

#### (3) References

None

### 13.1.2.1 Structure of the Bytes

#### (1) Basic Specifications

The length byte TL is followed by a variable number of optional subsequent bytes in the following order:

- format byte T0,
- interface bytes TA(1), TB(1), TC(1) and
- historical bytes T1 to Tk.

#### (2) Extended Specifications

None

#### (3) References

None

### 13.1.2.2 Length Byte

#### (1) Basic Specifications

The length byte TL is mandatory and specifies the length of the transmitted ATS including itself. The two CRC bytes are not included in TL. The maximum size of the ATS shall not exceed the indicated FSD. Therefore the maximum value of TL shall not exceed FSD-2.

#### (2) Extended Specifications

None

#### (3) References

None

### 13.1.2.3 Format Byte

#### (1) Basic Specifications

The format byte T0 is optional and is present as soon as the length is greater than 1. The ATS can only contain the following optional bytes when this format byte is present.

To consists of three parts (see "Fig. 13.1-5 Coding of Format Byte"):

- The most significant bit b8 shall be set to 0. The value 1 is RFU.
- The bits b7 to b5 contain Y(1) indicating the presence of subsequent interface bytes TC(1), TB(1) and TA(1).
- The least significant half byte b4 to b1 is called FSCI and codes FSC. The FSC defines the maximum size of a frame accepted by the PICC. The default value of FSCI is 2 and leads to a FSC of 32 bytes. The coding of FSC is equal to the coding of FSDI (see "Table 13.1-1 FSDI to FSD Conversion").

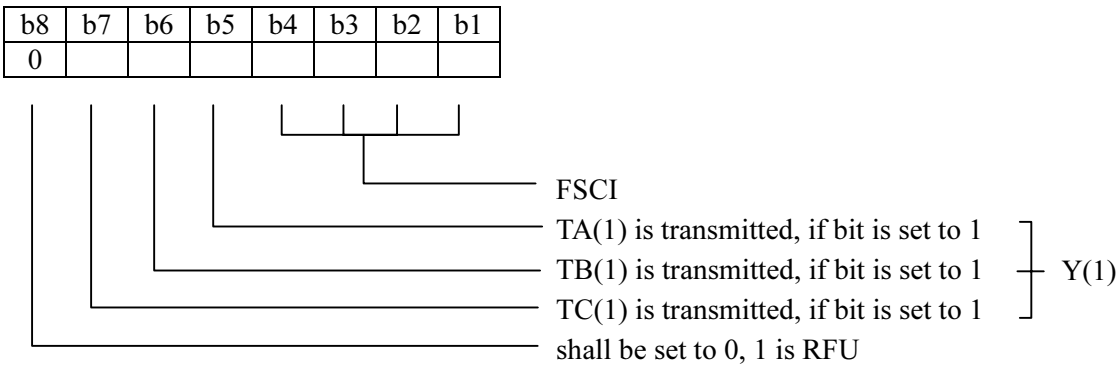


Fig. 13.1-5 Coding of Format Byte

#### (2) Extended Specifications

None

#### (3) References

None

### 13.1.2.4 Interface Byte TA(1)

#### (1) Basic Specifications

The interface byte TA(1) consists of four parts (see "Fig. 13.1-6 Coding of Interface byte TA (1)"):

- The most significant bit b8 codes the possibility to handle different divisors for each direction. When this bit is set to 1 the PICC is unable to handle different divisors for each direction.
- The bits b7 to b5 code the bit rate capability of the PICC for the direction from PICC to PCD, called DS. The default value shall be (000)b.
- The bit b4 shall be set to (0)b and the other value is RFU.
- The bits b3 to b1 code the bit rate capability of the PICC for the direction from PCD to PICC, called DR. The default value shall be (000)b.

b8	b7	b6	b5	b4	b3	b2	b1
				0			

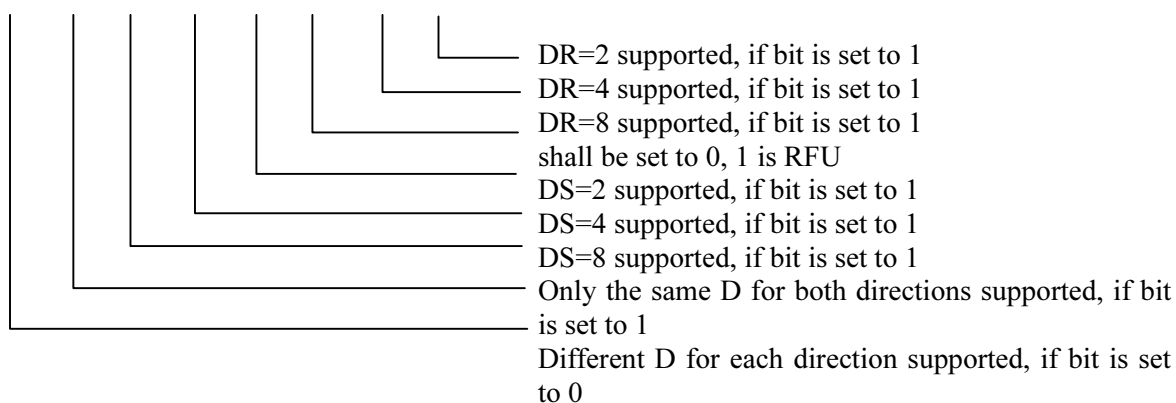


Fig. 13.1-6 Coding of Interface Byte TA(1)

The selection of a specific divisor D for each direction may be done by the PCD using a PPS.

#### (2) Extended Specifications

None

#### (3) References

None

### 13.1.2.5 Interface Byte TB(1)

#### (1) Basic Specifications

The interface byte TB(1) conveys information to define the frame waiting time and the start-up frame guard time.

The interface byte TB(1) consists of two parts (see "Fig. 13.1-7 Coding of interface byte TB(1)"):

- The most significant half-byte b8 to b5 is called FWI and codes FWT (see "13.3.2 Frame Waiting Time (FWT)"). The value of FWI may be from 0 to 14, and a value of 15 indicates RFU. The initial value of FWI is to be 4.
- The least significant half byte b4 to b1 is called SFGI and codes a multiplier value used to define the SFGT. The SFGT defines a specific guard time needed by the PICC before it is ready to receive the next frame after it has sent the ATS. SFGI is coded in the range from 0 to 14. The value of 15 is RFU. The value of indicates no SFGT needed and the values in the range from 1 to 14 are used to calculate the SFGT with the formula given below. The default value of SFGI is 0.

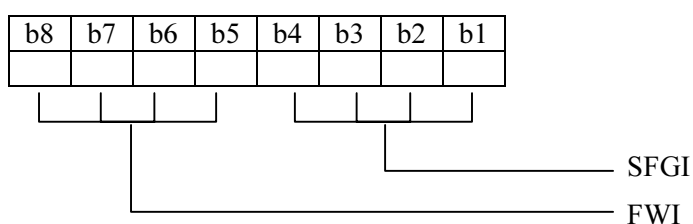


Fig. 13.1-7 Coding of Interface Byte TB(1)

SFGT is calculated by the following formula:

$$\text{SFGT} = (256 \times 16 / f_c) \times 2^{\text{SFGI}}$$

SFGTMIN = minimum value of the frame delay time as defined in "12.Anticollision"

SFGTDEFAULT = SFGTMIN

SFGTMAX = approx. 4949 ms

#### (2) Extended Specifications

None

#### (3) References

None

### 13.1.2.6 Interface Byte TC(1)

#### (1) Basic Specifications

The interface byte TC(1) specifies a parameter of the protocol.

The specific interface byte TC(1) consists of two parts (see "Fig. 13.1-8 Coding of interface byte TC(1)"):

- The most significant bits b8 to b3 shall be (000000)b and all other values are RFU.
- The bits b2 and b1 define which optional fields in the prologue field a PICC does support. The PCD is allowed to skip fields, which are supported by the PICC, but a field not supported by the PICC shall never be transmitted by the PCD. The default value shall be (10)b indicating CID supported and NAD not supported.

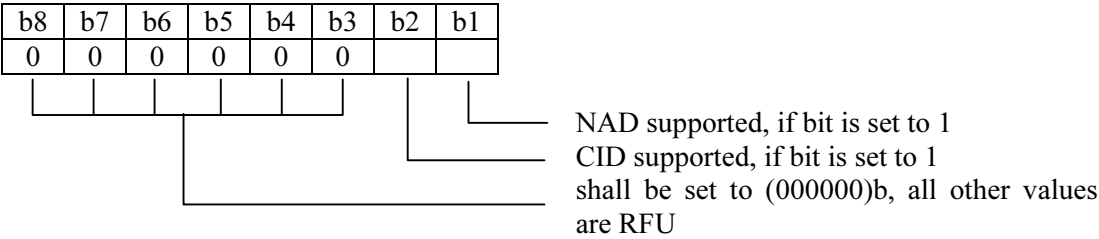


Fig. 13.1-8 Coding of Interface Byte TC(1)

#### (2) Extended Specifications

None

#### (3) References

None

### 13.1.2.7 Historical Bytes

#### (1) Basic Specifications

The historical bytes A1 to Ak are optional and designate general information. The maximum length of the ATS gives the maximum possible number of historical bytes. ISO/IEC 7816-4 specifies the content of the historical bytes.

#### (2) Extended Specifications

None

#### (3) References

None



### 13.1.3 Protocol and Parameter Selection Request

#### (1) Basic Specifications

PPS request contains the start byte that is followed by the format byte and parameter byte (see "Fig. 13.1-9 Protocol and parameter selection request").

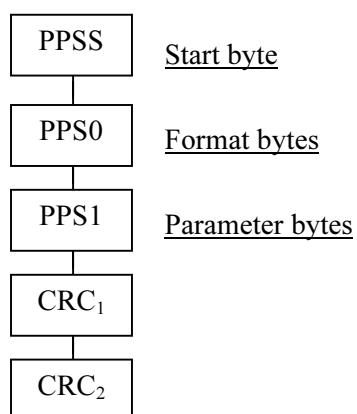


Fig. 13.1-9 Protocol and Parameter Selection Request

#### (2) Extended Specifications

None

#### (3) References

None

13.1.3.1 Protocol and Parameter Selection (PPS) Start

(1) Basic Specifications

The first byte of PPS is the start byte, and is called PPSS. PPSS consists of two parts (see "Fig. 13.1-10 Coding of PPSS"):

- The most significant half byte b8 to b5 shall be set to 'D' and identifies the PPS.
- The least significant half byte b4 to b1 is named CID and it defines the logical number of the addressed PICC.

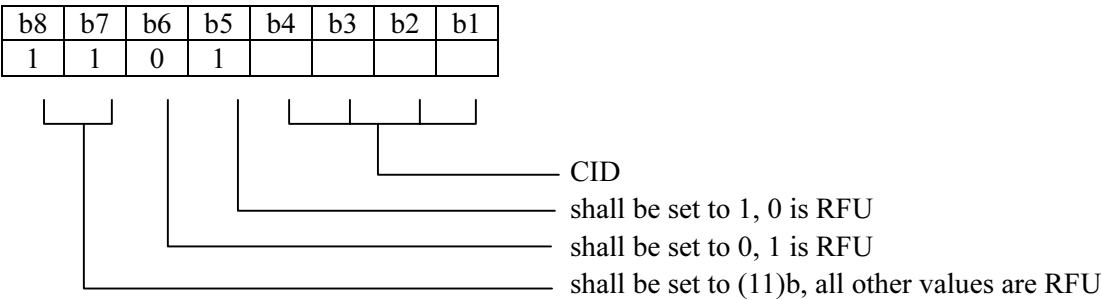


Fig. 13.1-10 Coding of PPSS

(2) Extended Specifications

None

(3) References

None

13.1.3.2 PPS0

(1) Basic Specifications

PPS0 indicates the presence of the optional byte PPS1 (see "Fig. 13.1-11 PPS0").

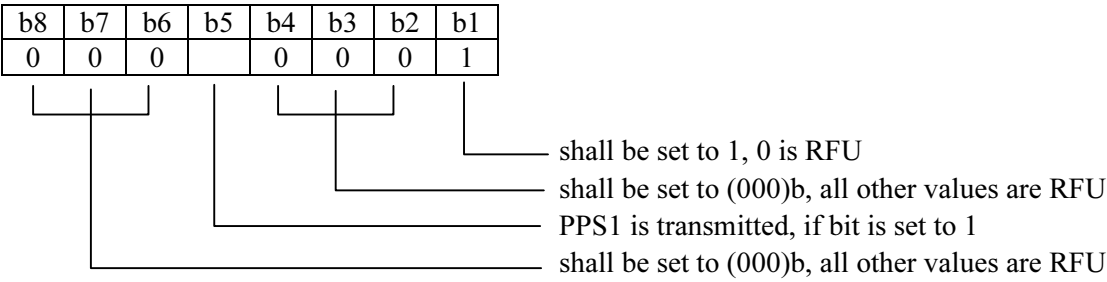


Fig. 13.1-11 Coding of PPSS0

(2) Extended Specifications

None

(3) References

None

### 13.1.3.3 PPS1

#### (1) Basic Specifications

PPPS1 consists of three parts (see "Fig. 13.1-12 Coding of PPS1"):

- The most significant half byte b8 to b5 shall be (0000)b and all other values are RFU.
- The bits b4 to b3 are called DSI and code the selected divisor integer from PICC to PCD.
- The bits b2 and b1 are called DRI and code the selected divisor integer from PCD to PICC.

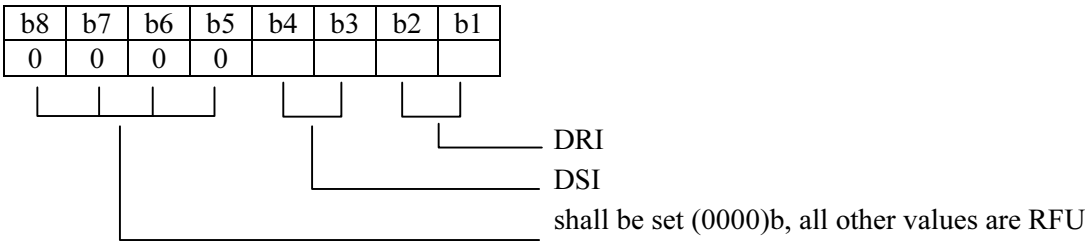


Fig. 13.1-12 Coding of PPS1

For the definition of DS and DR, see "13.1.2.4 Interface Byte TA(1)".

The coding of D is given in "Table 13.1-2 DRI, DSI to D conversion".

Table 13.1-2 DRI, DSI to D conversion

DI	(00)b	(01)b	(10)b	(11)b
D	1	2	4	8

#### (2) Extended Specifications

None

#### (3) References

None

### 13.1.4 Protocol and Parameter Selection Response

#### (1) Basic Specifications

The PPS response acknowledges the received PPS request and it contains only the start byte specified in "13.1.3.1 Protocol and Parameter Selection (PPS) Start". This structure of the PPS response is shown in "Fig. 13.1-13 Protocol and Parameter Selection Response".

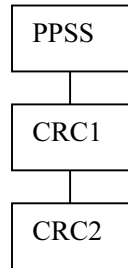


Fig. 13.1-13 Protocol and Parameter Selection Response

#### (2) Extended Specifications

None

#### (3) References

None

### 13.1.5 Activation Frame Waiting Time

#### (1) Basic Specifications

The activation frame waiting time defines the maximum time for a PICC to start sending its response frame after the end of a frame received from the PCD and has a value of  $65536/f_c$  ( $\sim 4833 \mu\text{s}$ ).

NOTE The minimum time between frames in any direction (from PCD to PICC and from PICC to PCD) is defined in "12. Anticollision".

#### (2) Extended Specifications

None

#### (3) References

None

### 13.1.6 Error Detection and Recovery

#### 13.1.6.1 Handling of RATS and ATS

##### (1) Basic Specifications

###### (a) PCD rules

When the PCD has sent the RATS and receives a valid ATS the PCD shall continue operation.

In any other case the PCD may retransmit the RATS or it shall use the deactivation sequence as defined in "13.4 Protocol Deactivation of PICC Type A and Type B".

###### (b) PICC rules

When the PICC has been selected with the last command and

1) receives a valid RATS, the PICC

- shall send back its ATS and
- shall disable the RATS (stop responding to received RATS).

2) receives any other block valid or invalid, except a HLTA Command, the PICC

- shall ignore the block and
- shall remain in receive mode.

##### (2) Extended Specifications

None

##### (3) References

None

### 13.1.6.2 Handling of PPS Request and PPS Response

#### (1) Basic Specifications

##### (a) PCD rules

When the PCD has sent a PPS request and received a valid PPS response the PCD shall activate the selected parameters and continue operation.

In any other case the PCD may retransmit a PPS request and continue operation.

##### (b) PICC rules

When the PICC has received a RATS, sent its ATS and

1) received a valid PPS request, the PICC

- shall send the PPS response,
- shall disable the PPS request (stop responding to received PPS requests) and
- shall activate the received parameter.

2) received an invalid block, the PICC

- shall disable the PPS request (stop responding to received PPS requests) and
- shall remain in receive mode.

3) received a valid block, except a PPS request, the PICC

- shall disable the PPS request (stop responding to received PPS requests) and
- shall continue operation.

#### (2) Extended Specifications

None

#### (3) References

None



### 13.1.6.3 Handling of the CID During Activation

#### (1) Basic Specifications

When the PCD has sent a RATS containing a CID not equal to 0 and

1) received an ATS indicating CID is supported, the PCD

- shall send blocks containing CID=n to this PICC and
- shall not use the CID=n for further RATS while this PICC is in ACTIVE state.

2) received an ATS indicating CID is not supported, the PCD

- shall send blocks containing no CID to this PICC and
- shall not activate any other PICC while this PICC is in ACTIVE state.

When the PCD has sent a RATS containing a CID equal to 0 and

1) received an ATS indicating CID is supported, the PCD

- may send blocks containing CID equal to 0 to this PICC and
- shall not activate any other PICC while this PICC is in ACTIVE state.

2) received an ATS indicating CID is not supported, the PCD shall

- send blocks containing no CID to this PICC and
- not activate any other PICC while this PICC is in ACTIVE state.

#### (2) Extended Specifications

None

#### (3) References

None

## 13.2 Protocol Activation of PICC Type B

### (1) Basic Specifications

The activation sequence for a PICC Type B is described in "12. Anticollision".

### (2) Extended Specifications

None

### (3) References

None

### 13.3 Half-duplex Block Transmission Protocol

#### (1) Basic Specifications

The half-duplex block transmission protocol addresses the special needs of contactless card environments and uses the frame format as defined in "12. Anticollision". Here, the following frame structures are specified.

- Data block

In addition, the following codings are specified.

- Flow control, block chaining and transmission control including error recovery, etc.
- Special interface control
- This protocol is designed according to the principle layering of the OSI reference model, with particular attention to the minimization of interactions across boundaries. Four layers are defined:
  - Physical layer exchanges bytes according to "12. Anticollision".
  - Data link layer exchanges blocks as defined in this clause.
  - Session layer combined with the data link layer for a minimum overhead.
  - Application layer processing commands, which involve the exchange of at least one block or chain of blocks in either direction.

#### (2) Extended Specifications

None

#### (3) References

None

13.3.1 Block Format

(1) Basic Specifications

The block format (see "Fig. 13.3-1 Block Format") consists of a prologue field (mandatory), an information field (optional) and an epilogue field (mandatory).

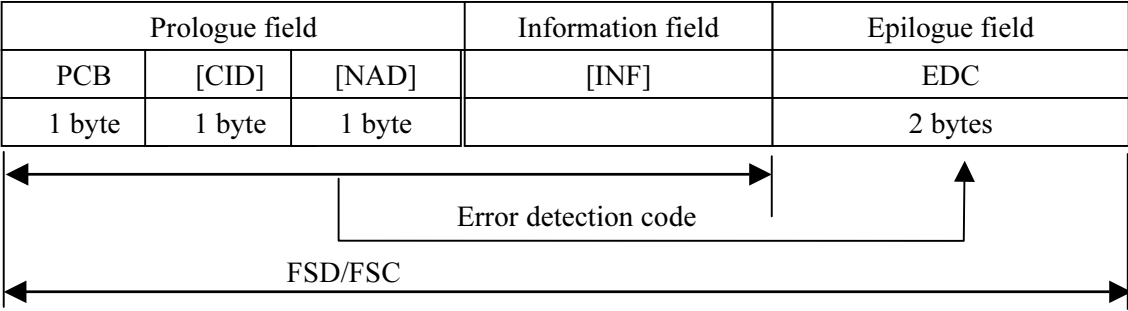


Fig. 13.3-1 Block Format

(2) Extended Specifications

None

(3) References

None

### 13.3.1.1 Prologue Field

#### (1) Basic Specifications

The prologue field is mandatory and consists of up to three bytes:

- Protocol Control Byte (mandatory),
- Card IDentifier (optional),
- Node ADdress (optional).

#### (a) Protocol Control Byte Field

The PCB is used to convey the information required to control the data transmission.

The protocol defines three fundamental types of blocks:

- I-Block used to convey information for use by the application layer.
- R-Block used to convey positive or negative acknowledgements. An R-Block never contains an INF field. The acknowledgement relates to the last received block.
- S-Block used to exchange control information between the PCD and the PICC.

Two different types of S-Blocks are defined:

- 1) Waiting time extension containing a 1 byte long INF field and
- 2) DESELECT containing no INF field

The coding of the PCB depends on its type and is defined by the following figures. PCB coding not defined here are either used in ISO/IEC 14443 or are RFU. The coding of I-Blocks, R-Blocks and S-Blocks are shown in "Fig. 13.3-2 Coding of I-Block PCB", "Fig. 13.3-3 Coding of R-Block PCB" and "Fig. 13.3-4 Coding of S-Block PCB".

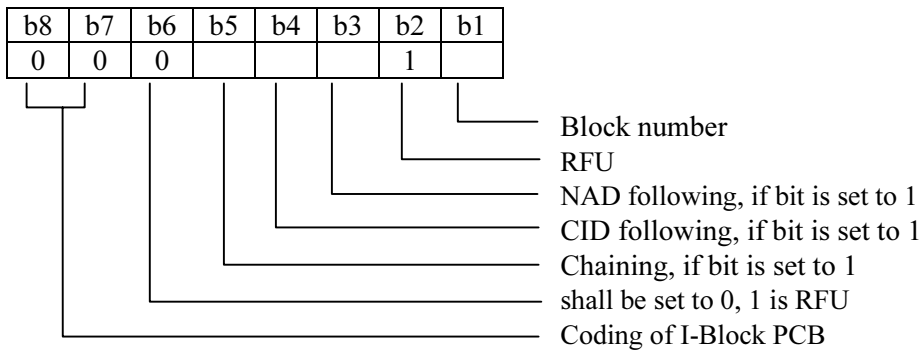


Fig. 13.3-2 Coding of I-Block PCB

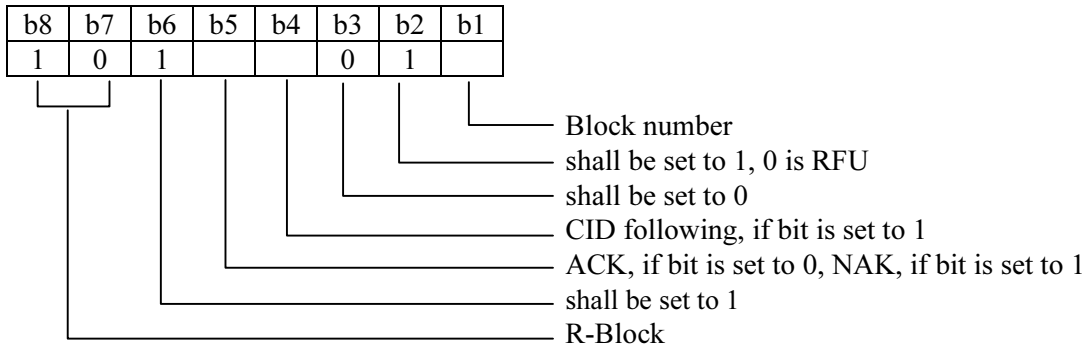


Fig. 13.3-3 Coding of R-Block PCB

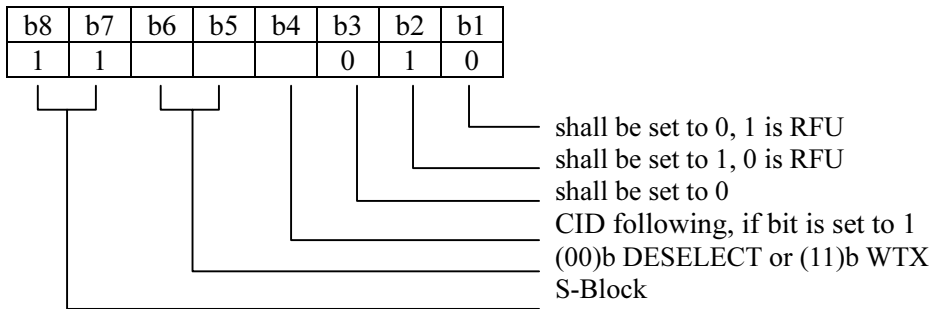


Fig. 13.3-4 Coding of S-Block PCB

## (b) Card Identifier Field

The CID field is used to identify a specific PICC and consists of three parts (see "Fig. 13.3-5 Coding of card identifier"):

- The two most significant bits b8 and b7 are used to indicate the power level indication received by a PICC from a PCD. There two bits shall be set to (00)b for PCD to PICC communication.
- The bits b6 and b5 are used to convey additional information, which are not defined and shall be set to (00)b and all other values are RFU.
- The bits b4 to b1 code the CID.

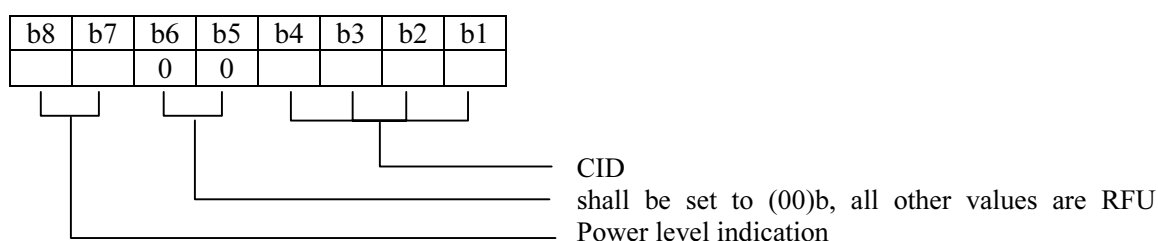


Fig. 13.3-5 Coding of Card Identifier

See "13.3.3 Power Level Indication" for specifications regarding power level indication. The coding of CID is given in "13.1.1 Request for Answer To Select" for Type A and "12. Anticollision" for Type B.

The handling of the CID by a PICC is described below:

A PICC, which does not support a CID

- shall ignore any block containing a CID.

A PICC, which does support a CID

- shall respond to blocks containing its CID by using its CID,
- shall ignore blocks containing other CIDs and
- shall, in case its CID is 0, respond also to blocks containing no CID by using no CID.

(c) Node Address Field

The NAD in the prologue field is reserved to build up and address different logical connections. The usage of the NAD shall be compliant with the definition from ISO/IEC 7816-3, when the bits b8 and b4 are both set to 0. All other values are RFU.

The following definitions shall apply for the usage of the NAD:

- a) The NAD field shall only be used for I-Blocks.
- b) When the PCD uses the NAD, the PICC shall also use the NAD,
- c) During chaining the NAD shall only be transmitted in the first block of chain,
- d) The PCD shall never use the NAD to address different PICCs (The CID shall be used to address different PICCs).
- e) When the PICC does not support the NAD, it shall ignore any block containing the NAD.

(2) Extended Specifications

None

(3) References

None



### 13.3.1.2 Information Field (INF)

#### (1) Basic Specifications

The INF field is optional. When present, the INF field conveys either application data in I-Blocks or non-application data and status information in S-Blocks. The length of the information field is calculated by counting the number of bytes of the whole block minus length of prologue and epilogue field.

#### (2) Extended Specifications

None

#### (3) References

None

### 13.3.1.3 Epilogue Field

#### (1) Basic Specifications

The epilogue field contains the EDC of the transmitted block, which is the CRC defined in "12. Anticollision".

#### (2) Extended Specifications

None

#### (3) References

None

### 13.3.2 Frame Waiting Time (FWT)

#### (1) Basic Specifications

The FWT defines the maximum time within which a PICC shall start its response frame after the end of a PCD frame (see "Fig. 13.3-6 Frame Waiting Time").

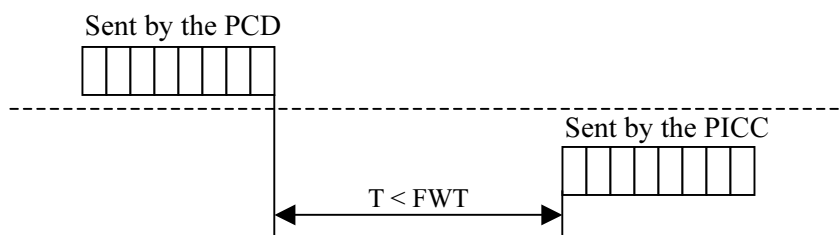


Fig. 13.3-6 Frame Waiting Time

NOTE The minimum time between frames in any direction is defined in "12. Anticollision".

FWT is calculated by the following formula:

$$FWT = (256 \times 16 / f_c) \times 2^{FWI}$$

$$FWT^{\text{MIN}} = \text{approx. } 302 \mu\text{s}$$

$$FWT^{\text{DEFAULT}} = \text{approx. } 4833 \mu\text{s}$$

$$FWT^{\text{MAX}} = \text{approx. } 4949 \text{ ms}$$

The FWT value shall be used by the PCD to detect a protocol error or an unresponsive PICC. The PCD obtains the right to re-transmit if the start of a response from the PICC is not received within FWT.

When the PICC needs more time than the defined FWT to process the received block it shall use an S(WTX) request for a waiting time extension. An S(WTX) request contains a 1 byte long INF field that consists of two parts (see "Fig. 13.3-7 Coding of INF field of an S(WTX) Request"):

- The two most significant bits b8 and b7 code the power level indication (see "13.3.3 Power Level Indication").
- The least significant bits b6 to b1 code the WTXM. The WTXM is coded in the range from 1 to 59. The values 0 and 60 to 63 are RFU.

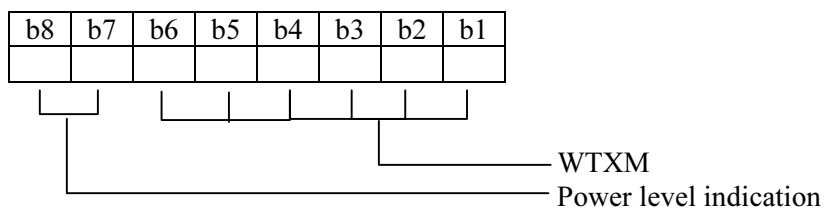


Fig. 13.3-7 Coding of INF Field of an S(WTX) Request

The PCD shall acknowledge by sending an S(WTX) response containing also a 1 byte long INF field that consists of two parts (see "Fig. 13.3-8 Coding of INF Field of an S(WTX) Response") and contains the same WTXM as received in the request:

- The most significant bits b8 and b7 shall be (00)b and all other values are RFU.
- The least significant bits b6 to b1 codes the acknowledged WTXM value used to define a temporary FWT.

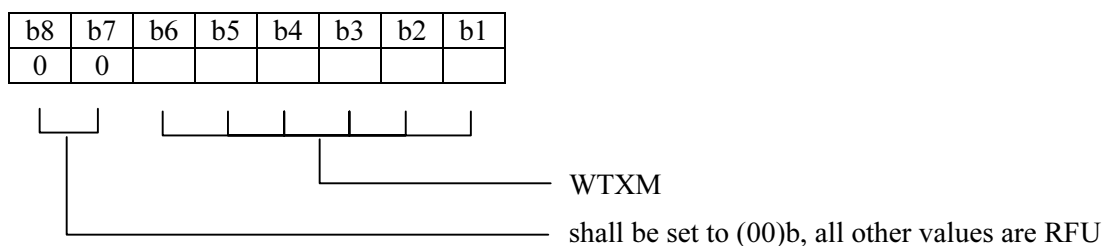


Fig. 13.3-8 Coding of INF Field of an S(WTX) Response

The corresponding temporary value of FWT is calculated by the following formula:

$$FWT^{\text{TEMP}} = FWT \times WTXM$$

The time  $FWT^{\text{TEMP}}$  requested by the PICC, starts after the PCD has sent the S(WTX) response.

$FWT^{\text{MAX}}$  shall be used, when the formula results in a value higher than  $FWT^{\text{MAX}}$ .

The temporary FWT applies only until the next block has been received by the PCD.

Type B FWI are included in ATQB (specified in "12. Anticollision").

In addition, type A FWI are included in ATS (specified in "13.1.2.5 Interface Byte TB(1)").

(2) Extended Specifications

None

(3) References

None

### 13.3.3 Power Level Indication

#### (1) Basic Specifications

The power level indication is coded as shown in "Table 13.3-1 Coding of Power Level Indication" using two bits embedded in the CID field (when present) and in the S-Block sent by the PICC (see "13.3.1.1(b) Card Identifier Field" and "13.3.2 Frame Waiting Time (FWT)"). When coding the power level, the two bits contained in the CID (when present) and S-Block returned by the PICC are used.

Table 13.3-1 Coding of Power Level Indication

(00)b	PICC does not support the power level indication
(01)b	Insufficient power for full functionality
(10)b	Sufficient power for full functionality
(11)b	More than sufficient power for full functionality

#### (2) Extended Specifications

None

#### (3) References

Even if the PICC indicates a value other than (00)b, the PCD may ignore that indication.

### 13.3.4 Protocol Operation

#### (1) Basic Specifications

After the activation sequence the PICC shall wait for a block as only the PCD has the right to send. After sending a block, the PCD shall switch to receive mode and wait for a block before switching back to transmit mode.

The PICC may transmit blocks only in response to received blocks (it is insensitive to time delays). After responding, the PICC shall return to the receive mode.

The PCD shall not initiate a new pair of command / response until the current pair of command / response has been completed or if the frame waiting time is exceeded with no response.

#### (2) Extended Specifications

None

#### (3) References

None

### 13.3.4.1 Multi-Activation

#### (1) Basic Specifications

The Multi-Activation feature allows the PCD to hold several PICCs in the ACTIVE state simultaneously. It allows switching directly between several PICCs without needing additional time for deactivation of a PICC and activation of another PICC.

For an example of Multi-Activation, see "13.5 Multi-Activation Example".

NOTE The PCD needs to handle a separate block number for each activated PICC.

#### (2) Extended Specifications

None

#### (3) References

None



### 13.3.4.2 Chaining

#### (1) Basic Specifications

The chaining feature allows the PCD or PICC to transmit information that does not fit in a single block as defined by FSC or FSD respectively, by dividing the information into several blocks. Each of those blocks shall have a length less than or equal to FSC or FSD respectively.

The chaining bit in the PCB of an I-Block controls the chaining of blocks. Each I-Block with the chaining bit set shall be acknowledged by an R-Block.

The chaining feature is shown in "Fig. 13.3-9 Chaining" using a 16 bytes long string transmitted in three blocks.

Notation:

I(1)x        I-Block with chaining bit set and block number x

I(0)x        I-Block with chaining bit not set (last block of chain) and block number x

R(ACK)x    R-Block that indicates a positive acknowledge.

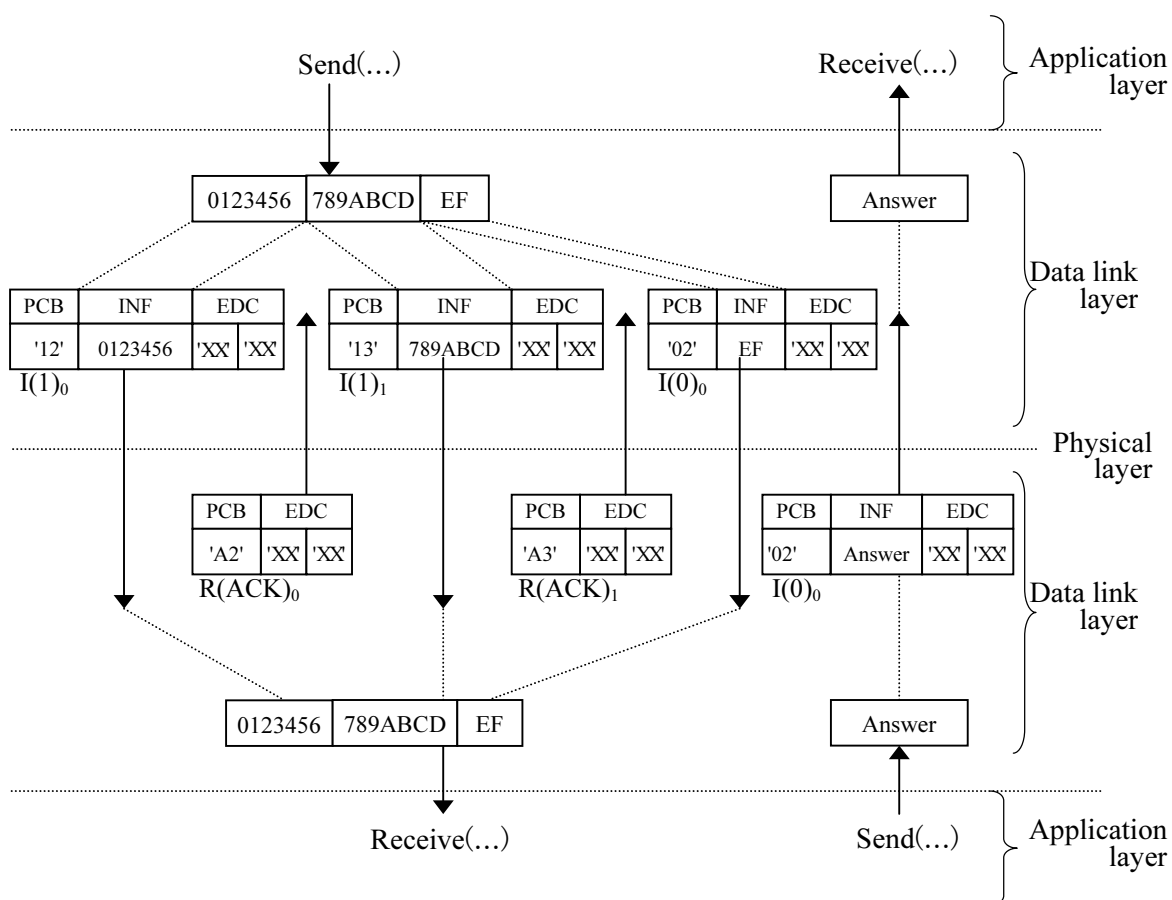


Fig. 13.3-9 Chaining

Note: This example does not use the optional fields NAD and CID.

## (2) Extended Specifications

None

## (3) References

None

### 13.3.4.3 Error Detection and Recovery

#### (1) Basic Specifications

The definitions made in clause overrule the block numbering rules (see "13.3.4.4 Block Number Rules").

The following errors shall be detected by the PCD:

##### 1) Transmission error (Frame error or EDC error) or FWT time-out

The PCD shall attempt error recovery by the following techniques in the order shown:

- Resends block (optional),
- Use of S(DESELECT) request,
- Ignore the PICC.

##### 2) Protocol error (infringement of PCB coding or infringement of protocol rules)

The PCD shall attempt error recovery by the following techniques in the order shown:

- Use of S(DESELECT) request,
- Ignore the PICC.

The following errors shall be detected by the PICC:

- Transmission error (Frame error or EDC error),
- Protocol error (infringement of the protocol rules).

The PICC shall attempt no error recovery. The PICC shall always return to receive mode, when a transmission error or a protocol error occurs and it shall accept an S(DESELECT) request at any time.

NOTE An R(NAK) block is never sent by the PICC.

#### (2) Extended Specifications

None

#### (3) References

None

#### 13.3.4.4 Block Number Rules

##### (1) Basic Specifications

###### (a) PCD Rules

Rule A: The PCD block number shall be initialized to 0 for each activated PICC.

Rule B: When an I-Block or an R(ACK) block with a block number equal to the current block number is received, the PCD shall toggle the current block number for that PICC before optionally sending a block.

###### (b) PICC Rules

Rule C: The PICC block number shall be initialized to 1 at activation.

Rule D: When an I-Block is received (independent of its block number), the PICC shall toggle its block number before sending a block.

Rule E: When an R(ACD) block with a block number not equal to the current PICC's block number is received, the PICC shall toggle its block number before sending a block.

##### (2) Extended Specifications

None

##### (3) References

None

### 13.3.4.5 Block Handling Rules

#### (1) Basic Specifications

##### (a) General Rules

- Rule 1: The first block shall be sent by the PCD.
- Rule 2: When an I-Block indicating chaining is received, the block shall be acknowledged by an R(ACK) block.
- Rule 3: S-Blocks are only used in pairs. An S(...) request block shall always be followed by an S(...) response block (see "13.3.2 Frame Waiting Time (FWT)" and "13.4 Protocol Deactivation of PICC Type A and Type B").

##### (b) PCD Rules

- Rule 4: When an invalid block is received or a FWT time-out occurs, an R(NAK) block shall be sent (except in the case of PICC chaining or S(DESELECT)).
- Rule 5: In the case of PICC chaining, when an invalid block is received or a FWT time-out occurs, an R(ACK) block shall be sent.
- Rule 6: When an R(ACK) block is received, if its block number is not equal to the PCD's current block number, the last I-Block shall be re-transmitted.
- Rule 7: When an R(ACK) block is received, if its block number is equal to the PCD's current block number, chaining shall be continued.
- Rule 8: If the S(Deselect) request is not answered by an error-free S(DESELECT) response the S(DESELECT) request may be re-transmitted or the PICC may be ignored.

##### (c) PICC Rules

- Rule 9: The PICC is allowed to send an S(WTX) block instead of an I-Block or an R(ACK) block.
- Rule 10: When an I-Block not indicating chaining is received, the block shall be acknowledged by an I-Block.
- Rule 11: When an R(ACK) or an R(NAK) block is received, if its block number is equal to the PICC's current block number, the last block shall be re-transmitted.

Rule 12: When an R(NAK) block is received, if its block number is not equal to the PICC's current block number, an R(ACK) block shall be sent.

Rule 13: When an R(ACK) block is received, if its block number is not equal to the PICC's current block number, and the PICC is in chaining, chaining shall be continued.

(2) Extended Specifications

None

(3) References

None

## 13.4 Protocol Deactivation of PICC Type A and Type B

### (1) Basic Specifications

The PICC shall be set to the HALT state, after the transactions between PCD and PICC have been completed.

The deactivation of a PICC is done by using a DESELECT Command.

The DESELECT Command is coded as an S-Block of the protocol and consists of an S(DESELECT) request block sent by the PCD and an S(DESELECT) response sent as acknowledge by the PICC.

### (2) Extended Specifications

None

### (3) References

None

### 13.4.1 Deactivation Frame Waiting Time

#### (1) Basic Specifications

The deactivation frame waiting time defines the maximum time for a PICC to start sending its S(DESELECT) response frame after the end of the S(DESELECT) request frame received from the PCD and has a value of  $65536/f_c$  (= approx. 4833  $\mu$ s).

Note: The minimum time between frames in any direction is defined in "12. Anticollision".

#### (2) Extended Specifications

None

#### (3) References

None



### 13.4.2 Error Detection and Recovery

#### (1) Basic Specifications

When the PCD has sent an S(DESELECT) request and has received an S(DESELECT) response, the PICC has been set successfully to the HALT state and the CID assigned to it is released.

When the PCD fails to receive an S(DESELECT) response the PCD may retry the deactivation sequence.

#### (2) Extended Specifications

None

#### (3) References

None

### 13.5 Multi-Activation Example

#### (1) Basic Specifications

The following table describes an example of the usage of Multi-Activation for three PICCs.

Table 13.5-1 Multi-Activation

PCD Action	Status PICC 1	Status PICC 2	Status PICC 3
Power On field	-	-	-
Three PICC enter the field	IDLE	IDLE	IDLE
Activate PICC with CID=1	ACTIVE(1)	IDLE	IDLE
Any data transmission with CID=1	ACTIVE(1)	IDLE	IDLE
...	-	-	-
Activate PICC with CID=2	ACTIVE(1)	ACTIVE(2)	IDLE
Any data transmission with CID=1,2	ACTIVE(1)	ACTIVE(2)	IDLE
...			
Activate PICC with CID=3	ACTIVE(1)	ACTIVE(2)	ACTIVE(3)
Any data transmission with CID=1,2,3	ACTIVE(1)	ACTIVE(2)	ACTIVE(3)
...	-	-	-
S(DESELECT) Command with CID=3	ACTIVE(1)	ACTIVE(2)	HALT
S(DESELECT) Command with CID=2	ACTIVE(1)	HALT	HALT
S(DESELECT) Command with CID=1 HALT	HALT	HALT	HALT
...	-	-	-

#### (2) Extended Specifications

None

#### (3) References

None

## 13.6 Protocol Scenarios

### (1) Basic Specifications

This annex gives some scenarios for an error-free operation as well as for error handling. These scenarios may be used to build test cases for compliance tests.

The following symbols are used.

All block	==>	correctly received
All block	≠=>	erroneously received
All block	==>	nothing received (FWT time-out)
Separation line	___	end of the smallest protocol operation
I(1)x		I-Block with chaining bit set and block number x
I(0)x		I-Block with chaining bit not set (last block of chain) and block number x
R(ACK)x		R-Block indicating a positive acknowledge
R(NAK)x		R-Block indicating a negative acknowledge
S(...)		S-Block

The block numbering in a scenario always starts with the PCD's current block number for the destination PICC. For ease of presentation, scenarios start after the PICC activation sequence and hence the current block numbers start with 0 for the PCD and with 1 for the PICC.

"Fig. 13.6-1 Exchange of I-Blocks"  
"Fig. 13.6-2 Request for Waiting Time Extension"  
"Fig. 13.6-3 DESELECT"  
"Fig. 13.6-4 Chaining (Part 1)"  
"Fig. 13.6-5 Chaining (Part 2)"  
"Fig. 13.6-6 Exchange of I-Blocks (Part 1)"  
"Fig. 13.6-7 Exchange of I-Blocks (Part 2)"  
"Fig. 13.6-8 Exchange of I-Blocks (Part 3)"  
"Fig. 13.6-9 Exchange of I-Blocks (Part 4)"  
"Fig. 13.6-10 Request for Waiting Time Extension (Part 1)"  
"Fig. 13.6-11 Request for Waiting Time Extension (Part 2)"  
"Fig. 13.6-12 Request for Waiting Time Extension (Part 3)"  
"Fig. 13.6-13 Request for Waiting Time Extension (Part 4)"  
"Fig. 13.6-14 Request for Waiting Time Extension (Part 5)"  
"Fig. 13.6-15 DESELECT"  
"Fig. 13.6-16 Chaining (Part 1)"  
"Fig. 13.6-17 Chaining (Part 2)"  
"Fig. 13.6-18 Chaining (Part 3)"  
"Fig. 13.6-19 Chaining (Part 4)"  
"Fig. 13.6-20 Chaining (Part 5)"  
The scenario examples are shown above.

## (2) Extended Specifications

None

## (3) References

None

13.6.1 Error-free Operation

13.6.1.1 Exchange of I-Blocks

(1) Basic Specifications

Scenario 1: Exchange of I-Blocks

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
	Rule 1		I(0)0	==>		0	Rule D
1	Rule B	1		<==	I(0)0		Rule 10
2			I(0)1	==>		1	Rule D
3	Rule B	0		<==	I(0)1		Rule 10

Fig. 13.6-1 Exchange of I-Blocks

(2) Extended Specifications

None

(3) References

None

### 13.6.1.2 Request for Waiting Time Extension

#### (1) Basic Specifications

Scenario 2: Waiting time extension

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		I(0)0	==>		0	Rule D
2				<==	S(WTX) request		Rule 9
3			S(WTX) response	==>			
4	Rule B	1		<==	I(0)0		Rule 10
5			I(0)1	==>		1	Rule D
6	Rule B	0		<==	I(0)1		Rule 10

Fig. 13.6-2 Request for Waiting Time Extension

#### (2) Extended Specifications

None

#### (3) References

None

13.6.1.3 DESELECT

(1) Basic Specifications

Scenario 3: DESELECT

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
7	Rule 1		I(0)0	==>		0	Rule D
8	Rule B	1		<==	I(0)0		Rule 10
9			S(DESELECT) request	==>		1	Rule D
10				<==	S(DESELECT) response		Rule 3

Fig. 13.6-3 DESELECT

(2) Extended Specifications

None

(3) References

None

## 13.6.1.4 Chaining

## (1) Basic Specifications

Scenario 4: PCD uses chaining

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(1)_0$	$\implies$		0	Rule D
2	Rule B	1		$\longleftarrow$	$R(ACK)_0$		Rule 2
3	Rule 7		$I(0)_1$	$\implies$		1	Rule D
4	Rule B	0		$\longleftarrow$	$I(0)_1$		Rule 10
5			$I(0)_0$	$\implies$		0	Rule D
6	Rule B	1		$\longleftarrow$	$I(0)_0$		Rule 10

Fig. 13.6-4 Chaining (Part 1)

Scenario 5: PICC uses chaining

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(0)_0$	$\implies$		0	Rule D
2	Rule B	1		$\longleftarrow$	$I(1)_0$		Rule 10
3	Rule 2		$R(ACK)_1$	$\implies$		1	Rule E
4	Rule B	0		$\longleftarrow$	$I(0)_1$		Rule 12
5			$I(0)_0$	$\implies$		0	Rule D
6	Rule B	1		$\longleftarrow$	$I(0)_0$		Rule 10

Fig. 13.6-5 Chaining (Part 2)

## (2) Extended Specifications

None

## (3) References

None



## 13.6.2 Error handling

## 13.6.2.1 Exchange of I-Blocks

## (1) Basic Specifications

## Scenario 6: Start of Protocol

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(0)_0$	$\Rightarrow$			
2	Time out			$\Leftarrow$			
3	Rule 4		$R(NAK)_0$	$\Rightarrow$			
4		No change		$\Leftarrow$	$R(ACK)_1$		Rule 12
5	Rule 6		$I(0)_0$	$\Rightarrow$		0	Rule D
6	Rule B	1		$\Leftarrow$	$I(0)_0$		Rule 10
7			$I(0)_1$	$\Rightarrow$		1	Rule D
8	Rule B	0		$\Leftarrow$	$I(0)_1$		Rule 10

Fig. 13.6-6 Exchange of I-Blocks (Part 1)

## Scenario 7: Exchange of I-Blocks

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(0)_0$	$\Rightarrow$		0	Rule D
2	Rule B	1		$\Leftarrow$	$I(0)_0$		Rule 10
3			$I(0)_1$	$\Rightarrow$			
4	Time out			$\Leftarrow$			
5	Rule 4		$R(NAK)_1$	$\Rightarrow$			
6		No change		$\Leftarrow$	$R(ACK)_0$		Rule 12
7	Rule 6		$I(0)_1$	$\Rightarrow$		1	Rule D
8	Rule B	0		$\Leftarrow$	$I(0)_1$		Rule 10
9			$I(0)_0$	$\Rightarrow$		0	Rule D
10	Rule B	1		$\Leftarrow$	$I(0)_0$		Rule 10

Fig. 13.6-7 Exchange of I-Blocks (Part 2)

## Scenario 8: Exchange of I-Blocks

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(0)_0$	$\Rightarrow$		0	Rule D
2				$\nRightarrow$	$I(0)_0$		Rule 10
3	Rule 4		$R(NAK)_0$	$\Rightarrow$			
4	Rule B	1		$\Leftarrow$	$I(0)_0$		Rule 11
5			$I(0)_1$	$\Rightarrow$		1	Rule D
6	Rule B	0		$\Leftarrow$	$I(0)_1$		Rule 10

Fig. 13.6-8 Exchange of I-Blocks (Part 3)

## Scenario 9: Exchange of I-Blocks

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(0)_0$	$\Rightarrow$		0	Rule D
2				$\nRightarrow$	$I(0)_0$		Rule 10
3	Rule 4		$R(NAK)_0$	$\Rightarrow$			
4	Time out			$\Leftarrow$	-		
5	Rule 4		$R(NAK)_0$	$\Rightarrow$			
6	Rule B	1		$\Leftarrow$	$I(0)_0$		Rule 11
7			$I(0)_1$	$\Rightarrow$		1	Rule D
8	Rule B	0		$\Leftarrow$	$I(0)_1$		Rule 10

Fig. 13.6-9 Exchange of I-Blocks (Part 4)

## (2) Extended Specifications

None

## (3) References

None

## 13.6.2.2 Waiting Time Extension

## (1) Basic Specifications

## Scenario 10: Request for waiting time extension

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(0)_0$	$\Rightarrow$		0	Rule D
2				$\neq$	S(WTX) request		Rule 9
3	Rule 4		$R(NAK)_0$	$\Rightarrow$			
4				$\Leftarrow$	S(WTX) request		Rule 11
5	Rule 3		S(WTX) response	$\Rightarrow$			
6	Rule B	1		$\Leftarrow$	$I(0)_0$		Rule 10
7			$I(0)_1$	$\Rightarrow$		1	Rule D
8	Rule B	0		$\Leftarrow$	$I(0)_1$		Rule 10

Fig. 13.6-10 Waiting Time Extension (Part 1)

## Scenario 11: Request for waiting time extension

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(0)_0$	$\Rightarrow$		0	Rule D
2				$\neq$	S(WTX) request		Rule 9
3	Rule 4		$R(NAK)_0$	$\neq$			
4	Time out			$\Leftarrow$	-		
5	Rule 4		$R(NAK)_0$	$\Rightarrow$			
6				$\Leftarrow$	S(WTX) request		Rule 11
7	Rule 3		S(WTX) response	$\Rightarrow$			
8	Rule B	1		$\Leftarrow$	$I(0)_0$		Rule 10
9			$I(0)_1$	$\Rightarrow$		1	Rule D
10	Rule B	0		$\Leftarrow$	$I(0)_1$		Rule 10

Fig. 13.6-11 Request for Waiting Time Extension (Part 2)

## Scenario 12: Request for Waiting Time Extension

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(0)_0$	$\Rightarrow$		0	Rule D
2				$\Leftarrow$	S(WTX) request		Rule 9
3	Rule 3		S(WTX) response	$\Rightarrow$			
4	Time out			$\Leftarrow$	-		
5	Rule 4		$R(NAK)_0$	$\Rightarrow$			
6				$\Leftarrow$	S(WTX) request		Rule 11
7	Rule 3		S(WTX) response	$\Rightarrow$			
8	Rule B	1		$\Leftarrow$	$I(0)_0$		Rule 10
9			$I(0)_1$	$\Rightarrow$		1	Rule D
10	Rule B	0		$\Leftarrow$	$I(0)_1$		Rule 10

Fig. 13.6-12 Request for Waiting Time Extension (Part 3)

## Scenario 13: Request for Waiting Time Extension

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(0)_0$	$\Rightarrow$		0	Rule D
2				$\Leftarrow$	S(WTX) request		Rule 9
3	Rule 3		S(WTX) response	$\Rightarrow$			
4				$\Leftarrow$	$I(0)_0$		Rule 10
5	Rule 4		$R(NAK)_0$	$\Rightarrow$			
6	Rule B	1		$\Leftarrow$	$I(0)_0$		Rule 11
7			$I(0)_1$	$\Rightarrow$		1	Rule D
8	Rule B	0		$\Leftarrow$	$I(0)_1$		Rule 10

Fig. 13.6-13 Request for Waiting Time Extension (Part 4)

## Scenario 14: Request for Waiting Time Extension

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(0)_0$	$\Rightarrow$		0	Rule D
2				$\Leftarrow$	S(WTX) request		Rule 9
3	Rule 3		S(WTX) response	$\Rightarrow$			
4				$\Leftarrow$	$I(0)_0$		Rule 10
5	Rule 4		$R(NAK)_0$	$\Rightarrow$			
6	Time out			$\Leftarrow$	-		
7	Rule 4		$R(NAK)_0$	$\Rightarrow$			
8	Rule B	1		$\Leftarrow$	$I(0)_0$		Rule 11
9		0	$I(0)_1$	$\Rightarrow$		1	Rule D
10	Rule B			$\Leftarrow$	$I(0)_1$		Rule 10

Fig. 13.6-14 Request for Waiting Time Extension (Part 5)

(2) Extended Specifications

None

(3) References

None

### 13.6.2.3 DESELECT

#### (1) Basic Specifications

##### Scenario 15: DESELECT

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
11	Rule 1		I(0) <sub>0</sub>	==>			Rule D
12	Rule B			<==	I(0) <sub>0</sub>		Rule 10
13			S(DESELECT) request	≠=>			
14	Time out			<==	-		
15	Rule 8		S(DESELECT) request	==>			
16				<==	S(DESELECT) response		Rule 3

Fig. 13.6-15 DESELECT

#### (2) Extended Specifications

None

#### (3) References

None

## 13.6.2.4 Chaining

## (1) Basic Specifications

Scenario 16: PCD uses chaining

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(1)_0$	$\Rightarrow$		0	Rule D
2				$\neq$	$R(ACK)_0$		Rule 2
3	Rule 4		$R(NAK)_0$	$\Rightarrow$			
4	Rule B	1		$\Leftarrow$	$R(ACK)_0$		Rule 11
5	Rule 7		$I(1)_1$	$\Rightarrow$		1	Rule D
6	Rule B	0		$\Leftarrow$	$R(ACK)_1$		Rule 2
7	Rule 7		$I(0)_0$	$\Rightarrow$		0	Rule D
8	Rule B	1		$\Leftarrow$	$I(0)_0$		Rule 10
9			$I(0)_1$	$\Rightarrow$		1	Rule D
10	Rule B	0		$\Leftarrow$	$I(0)_1$		Rule 10

Fig. 13.6-16 Chaining (Part 1)

Scenario 17: PCD uses chaining

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(1)_0$	$\Rightarrow$		0	Rule D
2	Rule B	1		$\Leftarrow$	$R(ACK)_0$		Rule 2
3	Rule 7		$I(1)_1$	$\neq$			
4	Time-out			$\Leftarrow$	-		
5	Rule 4		$R(NAK)_1$	$\Rightarrow$			
6		No change		$\Leftarrow$	$R(ACK)_0$		Rule 12
7	Rule 6		$I(1)_1$	$\Rightarrow$		1	Rule D
8	Rule B	0		$\Leftarrow$	$R(ACK)_1$		Rule 2
9	Rule 7		$I(0)_0$	$\Rightarrow$		0	Rule D
10	Rule B	1		$\Leftarrow$	$I(0)_0$		Rule 10
11			$I(0)_1$	$\Rightarrow$		1	Rule D
12	Rule B	0			$I(0)_1$		Rule 10

Fig. 13.6-17 Chaining (Part 2)

Scenario 18: PCD uses chaining

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(1)_0$	$\implies$		0	Rule D
2				$\nleftarrow$	$R(ACK)_0$		Rule 2
3	Rule 4		$R(NAK)_0$	$\nrightarrow$			
4	Time-out			$\longleftarrow$	-		
5	Rule 4		$R(NAK)_0$	$\implies$			Rule D
6	Rule B	1		$\longleftarrow$	$R(ACK)_0$		Rule 11
7	Rule 7		$I(1)_1$	$\implies$		1	Rule D
8	Rule B	0		$\longleftarrow$	$R(ACK)_1$		Rule 2
9	Rule 7		$I(0)_0$	$\implies$		0	Rule D
10	Rule B	1		$\longleftarrow$	$I(0)_0$		Rule 10
11			$I(0)_1$	$\implies$		1	Rule D
12	Rule B	0		$\longleftarrow$	$I(0)_1$		Rule 10

Fig. 13.6-18 Chaining (Part 3)

Scenario 19: PCD uses chaining

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(0)_0$	$\implies$		0	Rule D
2	Rule B	1		$\longleftarrow$	$I(1)_0$		Rule 10
3	Rule 2		$R(ACK)_1$	$\nrightarrow$			
4	Time-out			$\longleftarrow$	-		
5	Rule 5		$R(ACK)_1$	$\implies$		1	Rule E
6	Rule B	0		$\longleftarrow$	$I(1)_1$		Rule 13
7	Rule 2		$R(ACK)_0$	$\implies$		0	Rule E
8	Rule B	1		$\longleftarrow$	$I(0)_0$		Rule 13
9			$I(0)_1$	$\implies$		1	Rule D
10	Rule B	0		$\longleftarrow$	$I(0)_1$		Rule 10

Fig. 13.6-19 Chaining (Part 4)



## Scenario 20: PCD uses chaining

	Comment	Block no. (0)	PCD		PICC	Block no. (1)	Comment
1	Rule 1		$I(0)_0$	$\implies$		0	Rule D
2	Rule B	1		$\Leftarrow$	$I(1)_0$		Rule 10
3	Rule 2		$R(ACK)_1$	$\implies$		1	Rule D
4				$\Leftarrow \neq$	$I(1)_1$		Rule 12
5	Rule 5		$R(ACK)_1$	$\implies$		No change	
6	Rule B	0		$\Leftarrow$	$I(1)_1$		Rule 11
7	Rule 2		$R(ACK)_0$	$\implies$		0	Rule D
8	Rule B	1		$\Leftarrow$	$I(0)_0$		Rule 12
9			$I(0)_1$	$\implies$		1	Rule D
10	Rule B	0		$\Leftarrow$	$I(0)_1$		Rule 10

Fig. 13.6-20 Chaining (Part 5)

## (2) Extended Specifications

None

## (3) References

None

## 13.7 Block and Frame Coding Overview

### (1) Basic Specifications

"Table 13.7-1 Block and Frame Coding" gives an overview of the different block and frame coding sent by the PCD.

The type of a block respectively frame is indicated by the first byte.

#### (a) Definitions made in "12. Anticollision":

REQA	(0100110)b (7 bit)
WUPA	(1010010)b (7 bit)
REQB/WUPB	(00000101)b
SLOT MARKER (Type B only)	(xxxx0101)b
Select (Type A only)	(1001xxxx)b
ATTRIB (Type B only)	(00011101)b
HLTA	(01010000)b
HLTB	(01010000)b

#### (b) Definitions made in "13. Transmission Protocol":

RATS	(11100000)b	
PPS	(1101xxxx)b	
I-Block	(00xxxxxx)b	(not (00xxx101)b)
R-Block	(10xxxxxx)b	(not (1001xxx)b)
S-Block	(11xxxxxx)b	(not (1110xxxx)b or (1101xxxx)b)

Table 13.7-1 Block and Frame Coding

Bit	I-Block PCB	R-Block PCB	DESELECT S-Block PCB WTX		REQB / WUPB	SLOT MARKER	SELECT	ATTRIB	HLTA	HLTB	RATS	PPS
b8	0	1	1		0	X	1	0	0	0	1	1
b7	0	0	1		0	X	0	0	1	1	1	1
b6	0 (RFU)	1	0	1	X	X	0	0	0	0	1	0
b5	Chaining	ACK/NAK	0	1	X	X	1	1	1	1	0	1
b4	CID	CID	CID		0	X	X	1	0	0	0	X
b3	NAD	0 (no NAD)	0 (no NAD)		1	1	X	1	0	0	0	X
b2	1	1 (RFU)	1 (RFU)		0	0	X	0	0	0	0	X
b1	Block No.	Block No.	0 (RFU)		1	1	X	1	0	0	0	X

## (2) Extended Specifications

None

## (3) References

None

### 13.8 T=1 Protocol Usage Specifications

These specifications stipulate usage specifications in the case of applying the T=1 protocol specified in ISO/IEC 7816-3 to proximity contactless IC cards. The contents described in "13.8 T=1 Protocol Usage Specifications" are all "reference specifications".

In the past, although the T=1 protocol was used in PICC provided with pins, it has been requested that they would also like to be used in proximity contactless IC cards. However, since the T=1 protocol is targeted at a single PICC connected with a wire, it cannot be applied directly to multiple PICC. In addition, since the communication protocol employed in ISO/IEC has a different T=1 protocol and block format, in environments in which both PICC employing this protocol and PICC employing the T=1 protocol are present, there is the potential for interference. Therefore, the following stipulates usage specifications of a T=1 protocol that solves these problems and can be applied to contactless IC cards (hereafter, to be referred to as the T=1' protocol).

### 13.8.1 PICC Activation

The procedure for PICC activation shall follow the procedures described in "12. Anticollision" and "13. Transmission Protocol". However, some responses from the PICC are changed in order to indicate differences in the protocol.

#### (a) Changes in Type A Time Slot Activation

In the case of using the T=1' protocol, the response (SAK\_t) to an SEL\_t command is changed to that shown in "Fig. 13.8-1 SAK\_t Response Format during T=1 Protocol" (equivalent to ATR of ISO/IEC 7816-3). The PICC switches to the T=1' protocol after sending SAK\_t.

In the case a PICC is present that returns a response other than SAK\_t specified here or SAK\_t specified in "12. Anticollision", since this is not a PICC eligible for this standardization, a HALT\_t command is issued and the PICC is deactivated.

TS	T0	TA1	TB1	TC1	TD1	TA2	TB2	TC2	TD2	TA3	...	T1	...	Tk	CRC
----	----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	----	-----	----	-----

Fig. 13.8-1 SAK\_t Response Format during T=1 Protocol

TS: '3B' is to be fixed (LSB first, positive logic)

T0, Tai, Tbi, Tci, Tdi, T1...Tk: Same as ISO/IEC 7816-3 except for the following items:

T: Valid only when T=1, other values are taken to indicate RFU.

FI: FI = 128 regardless of value.

N, CWT: 8 etu regardless of value.

P, I, X, C: Values are invalid since this function does not exist.

Indication of protocol options: CRC is used regardless of value.

CRC: CRC of ISO/IEC 3309 is used (CRC initial value: 'FFFF').

(b) Changes in Type B Activation

In the case of using the T=1' protocol, some of the coding of the ATQB response and ATTRIB command is changed, and information equivalent to ATR is returned with an Answer to ATTRIB response. The PICC switches to the T=1' protocol after sending the Answer to ATTRIB response.

Changes during T=1 protocol:

- ATQB response  
Application Data (4 bytes): "T=1" is used as the code indicating the T=1' protocol.  
Protocol\_Type (4 bits): (0000)b since the protocol is not specified in ISO/IEC.
- ATTRIB command  
Parameter 3 (b4 b3 b2 b1): (0000)b since the protocol is not specified in ISO/IEC.  
Higher layer INF: Not used
- Answer to ATTRIB response  
Equivalent to ATR (details are the same as those for the Type A time slot type).

### 13.8.2 Protocol Processing

Protocol processing shall follow the specifications in ISO/IEC 7816-3. However, some of the processing is changed due to differences in the communication method and to prevent interference.

#### (a) Communication Format

The communication format of the PICC shall follow the specifications in "11. Polling" and "12. Anticollision". However, a portion of the communication format is changed due to differences in the communication method and to prevent interference, and these changes are shown in "Table 13.8-1 Communication Format". In addition, the EDC is taken to be CRC (ISO/IEC 3309) to ensure the reliability of communications.

Table 13.8-1 Communication Format

Protocol Item	ISO/IEC 7816-3 T=1 protocol	Type A Time slot T=1' protocol	Type B T=1' protocol
Modulation/ demodulation	None	ISO/IEC 14443-2 Type A	ISO/IEC 14443-2 Type B
Encoding	NRZ	ISO/IEC 14443-2 Type A	ISO/IEC 14443-2 Type B
Frame format	None	ISO/IEC 14443-3 Appendix C	ISO/IEC 14443-3 Type B
Synchronization method	Start-stop synchronization	(Clock synchronization)	Start-stop synchronization
Character format	Start: 1 bit Data: 8 bits Parity: Even Stop: 1 bit	Data: 8 bits	Start: 1 bit Data: 8 bits Stop: 1 bit

## (b) NAD Coding

Although NAD is inherently a byte that represents the node address of communication, it is used here as a PICC identifier (CID) and PCD identifier to prevent interference. In addition, since a Vpp pin is not present on proximity contactless IC cards, the control bit of the Vpp pin is also changed so as to be used as an identifier. The coding of NAD is shown in "Fig. 13.8-2 NAD Coding".

b8	b7	b6	b5	b4	b3	b2	b1
DAD (Destination Identifier)				SAD (Sender Identifier)			

Fig. 13.8-2 NAD Coding

The PICC identifier (CID) is to be the CID designated during PICC activation.

The PCD identifier is to be the SAD present in a command received error-free by the PICC during the start of the protocol.

## (c) Operational NAD Assignment Restrictions

According to ISO/IEC 7816-3, NAD is able to assume any value other than the same DAD and SAD (excluding '0'). However, during application to proximity contactless IC cards, operational restrictions are placed on the assignment of NAD in consideration of the possibility of the presence of both a PICC before activation and a PICC complying with the protocol described in "13. Transmission Protocol".

However, these restrictions do not restrict the functions of the PICC, but rather only restrict the PICC with respect to system operation.



## a) NAD Restrictions of the Type A Time Slot Type

Coding of the first byte of commands used with the type A time slot type is shown in "Fig. 13.8-3 NAD Restrictions of Type A Time Slot Type".

		Lower 4 bits															
Upper 4 bits		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	0			I-Block				I-Block		ID		I-Block				I-Block	
	1			I-Block				I-Block				HALT_t		(0~7)			
	2																
	3						(REQ)					HALT_t		(8~F)			
	4	SEL_t (0~7)															
	5																
	6	SEL_t (8~F)															
	7																
	8																
	9																
	A			R-Block								R-Block					
	B			R-Block								R-Block					
	C			S(DESEL)								S(DESEL)					
	D	PPS															
	E	RATS															
	F			S(WTX)								S(WTX)					

	Commands specified in "12. Anticollision"
	Commands specified in "13. Transmission Protocol"
	Collision of commands (but able to be distinguished due to different command sizes)

Fig. 13.8-3 NAD Restrictions of Type A Time Slot Type

As a general rule, although NAD can be assigned to the empty spaces of the above "Fig. 13.8-3 NAD Restrictions of Type A Time Slot Type", in order to ensure future expandability, the PCD identifier and PICC identifier shall assume the values shown below.

- PCD identifier: 'D'
- PICC identifier (CID): Value other than 'D' (and '5' is also preferably not used)

Here, the HALT command for a PICC in which CID = '5' and the T=1 protocol command for a PICC in which CID = '5' have the same first byte. Although they can be distinguished since the frame sizes of both are clearly different, it is preferable not to use CID = '5' in consideration of the possibility of a PICC being present that responds incorrectly.

## b) NAD Restrictions of the Type B Type

Coding of the first byte of commands used with the type B type is shown in "Fig. 13.8-4 NAD Restrictions of Type B Type".

		Lower 4 bits																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
Upper 4 bits	1			I-Block			REQB	I-Block				I-Block				I-Block		
	2			I-Block			Slot marker	I-Block				I-Block			ATTR	I-Block		
	3																	
	4																	
	5	HALT																
	6																	
	7																	
	8																	
	9																	
	A			R-Block									R-Block					
	B			R-Block									R-Block					
	C			S(DESEL)									S(DESEL)					
	D																	
	E																	
	F			S(WTX)									S(WTX)					

Commands specified in "12. Anticollision"

Commands specified in "13. Transmission Protocol"

Fig. 13.8-4 NAD Restrictions of Type B Type

In accordance with the above "Fig. 13.8-4 NAD Restrictions of Type B Type", the PCD identifier and PICC identifier shall assume the values shown below.

- PCD identifier: Value of '1', '4', '8', '9' or 'C'
- PICC identifier (CID): Value other than identifier used by PCD

### 13.8.2.1 PICC Receive Error Processing

According to ISO/IEC 7816-3, an R-Block is to be sent during an IC card receive error. In the case of PICC, however, since there is the possibility of judging a command to another PICC as being a receive error, it is necessary to prevent the PICC from returning a response during a PICC receive error.

At this time, communication sequence management of the PICC performs processing by assuming that there has been no reception.

### 13.8.2.2 Card Deactivation

The procedure for PICC deactivation shall follow the procedure described in "12. Anticollision". Consequently, the HALT (HALT\_t) command can still be recognized even after the PICC has switched to the T=1 protocol.

### 13.9 Transmission Control Matrix of T=CL Protocol (Reference)

A transmission control matrix is shown in "Table 13.9-1 PICC Transmission Control Matrix (for Upper Device)" and "Table 13.9-2 PCD (Upper Device) Transmission Control Matrix (for PICC)" to facilitate understanding. These are only shown for reference purposes, however.

Table 13.9-1 PICC Transmission Control Matrix (for Upper Device)

Event  Status	Receive I-Block (from PCD)				Receive R-Block (from PCD)				Receive S-Block (from PCD)		Receive error message	
	A No chaining I(0)0 received	B No chaining I(0)1 received	C Chaining I(1)0 received	D Chaining I(1)1 received	E R(ACK)0 received	F R(ACK)1 received	G R(NAK)0 received	H R(NAK)1 received	I Response S(WTK) received	J Request S(DESELECT) received	K Error message (PCB error)	L Error message (CRC error, EGT time out)
0: Protocol start state	Internal bn updated Rule 10 → 1 Send I(0)0 Rule 10 → 3 Send I(1)0 Send S(WTX) → 7		Internal bn updated Rule 2 Send R(ACK)0 → 5 Send S(WTX) → 7		— → *	— → *	Rule 12 → 6 Send R(ACK)1	— → *	— → *	Send response S(DESELECT) → End of current protocol processing	— → *	— → *
1: Receive wait state after sending I(0)0 (no chaining)	Internal bn updated Rule 10 → 2 Send I(0)1 Rule 10 → 4 Send I(1)1 Send S(WTX) → 7		Internal bn updated Rule 2 Send R(ACK)1 → 6 Send S(WTX) → 7		Rule 11 → 1 Resend final block I(0)0	— → *	Rule 11 → 1 Resend final block I(0)0	Rule 12 → 5 Send R(ACK)0				
2: Receive wait state after sending I(0)1 (no chaining)	Internal bn updated Rule 10 → 1 Send I(0)0 Rule 10 → 3 Send I(1)0 Send S(WTX) → 7		Internal bn updated Rule 2 Send R(ACK)0 → 5 Send S(WTX) → 7		— → *	Rule 11 → 2 Resend final block I(0)1	Rule 12 → 6 Send R(ACK)1	Rule 11 → 2 Resend final block I(0)1				
3: Receive wait state after sending I(1)0 (chaining)	— → *		— → *		Rule 11 → 3 Resend final block I(1)0	Internal bn updated Rule 13 Send I(0)1 → 2 Send I(1)1 → 4	Rule 11 → 3 Resend final block I(1)0	— → *				
4: Receive wait state after sending I(1)1 (chaining)					Internal bn updated Rule 13 Send I(0)0 → 1 Send I(1)0 → 3	Rule 11 → 4 Resend final block I(1)1	— → *	Rule 11 → 4 Resend final block I(1)1				

Table 13.9-1 PICC Transmission Control Matrix (for Upper Device) (continued)

Event  Status	Receive I-Block (from PCD)				Receive R-Block (from PCD)				Receive S-Block (from PCD)		Receive error message	
	A  No chaining I(0)0 received	B  No chaining I(0)1 received	C  Chaining I(1)0 received	D  Chaining I(1)1 received	E  R(ACK)0 received	F  R(ACK)1 received	G  R(NAK)0 received	H  R(NAK)1 received	I  Response S(WTK) received	J  Request S(DESELECT) received	K  Error message (PCB error)	L  Error message (CRC error, EGT time out)
5: Receive wait state after sending R(ACK)0	Internal bn updated Rule 10 → 2 Send I(0)1 Rule 10 → 4 Send I(1)1 Send S(WTX) → 7		Internal bn updated Rule 2 Send R(ACK)1 → 6 Send S(WTX) → 7		— → *		Rule 11 → 5 Resend final block R(ACK)0	Rule 12 → 5 Send R(ACK)0	— → *	Send response S(DESELECT) → end of current protocol processing	— → *	— → *
6: Receive wait state after sending R(ACK)1	Internal bn updated Rule 10 → 1 Send I(0)0 Rule 10 → 3 Send I(1)0 Send S(WTX) → 7		Internal bn updated Rule 2 Send R(ACK) 0 → 5 Send S(WTX) → 7				Rule 12 → 6 Send R(ACK)1	Rule 11 → 6 Resend final block R(ACK)1				
7: Receive wait state after sending S(WTX) request	— → *		— → *		— → *		Send request S(WTX) → 7 (Resend)		Command to be sent prior to changing to this state are sent followed by proceeding to its status			

Note 1: The number retained internally by the PICC for imparting a block number to the block to be sent next is to be referred to as the internal block number (internal bn).

Note 2: \*: Returns to immediately previous transmission status

Table 13.9-2 PCD (Upper Device) Transmission Control Matrix (for PICC)

Event        Status	Receive I-Block (from PCD)				Receive R-Block (from PCD)		Receive S-Block (from PCD)		Receive error message		
	A	B	C	D	E	F	G	H	I	J	K
	No chaining I(0)0 received	No chaining I(0)1 received	Chaining I(1)0 received	Chaining I(1)1 received	R(ACK)0 received	R(ACK)1 received	Request S(WTK) received	Response S(DESELEC T) received	Error message (PCB error)	Error message (CRC error, EGT time out)	FWT time out
0: Waiting for instructions from upper layer	—	—	—	—	—	—	—	—	—	—	—
1: Receive wait state after sending I(0)0 (no chaining) Expecting I-Block	Normal termination (n clear) → 0 Waiting for upper layer instructions	Block number violation → 0	Normal receiving (n clear) Rule 2 → 6	Block number violation → 0	Protocol error → 0		Send response S(WTX)	Protocol error → 0	Format error → 0	Transmission error n+1 N = n-1: Retry out → 0 N > n-1: Rule 4 → 7	Transmission error n+1 N = n-1: Retry out → 0 N > n-1: Rule 4 → 7
2: Receive wait state after sending I(0)1 (no chaining) Expecting I-Block	Block number violation → 0	Normal termination (n clear) → 0 Waiting for upper layer instructions	Block number violation → 0	Normal termination (n clear) Rule 2 → 5						Transmission error n+1 N = n-1: Retry out → 0 N > n-1: Rule 4 → 8	Transmission error n+1 N = n-1: Retry out → 0 N > n-1: Rule 4 → 8
3: Receive wait state after sending I(1)0 (chaining) Expecting I-Block Expecting R(ACK)	Protocol error → 0				Chaining continued (n clear) Rule 7 Send I(0)1 → 2 Send I(1)1 → 4	Block number violation → 0				Transmission error n+1 N = n-1: Retry out → 0 N > n-1: Rule 4 → 8	Transmission error n+1 N = n-1: Retry out → 0 N > n-1: Rule 4 → 8
4: Receive wait state after sending I(1)1 (chaining) Expecting I-Block Expecting R(ACK)						Block number violation → 0				Chaining continued (n clear) Rule 7 Send I(0)1 → 1 Send I(1)1 → 3	Transmission error n+1 N = n-1: Retry out → 0 N > n-1: Rule 4 → 8
5: Receive wait state after sending R(ACK)0 Expecting I-Block	Normal termination (n clear) → 0 Chaining completed, waiting for upper layer instructions	Block number violation → 0	Chaining continued (n clear) Rule 2 → 6 Send R(ACK)1	Block number violation → 0	Protocol error → 0						

Table 13.9-2 PCD (Upper Device) Transmission Control Matrix (for PICC) (continued)

Event          Status	Receive I-Block (from PCD)				Receive R-Block (from PCD)		Receive S-Block (from PCD)		Receive error message		
	A	B	C	D	E	F	G	H	I	J	K
	No chaining I(0)0 received	No chaining I(0)1 received	Chaining I(1)0 received	Chaining I(1)1 received	R(ACK)0 received	R(ACK)1 received	Request S(WTK) received	Response S(DESELECT) received	Error message (PCB error)	Error message (CRC error, EGT time out)	FWT time out
6: Receive wait state after sending R(ACK)1 Expecting I-Block	Block number violation → 0	Normal termination (n clear) → 0 PICC chaining completed, waiting for upper layer instructions	Block number violation → 0	Chaining continued (n clear) Rule 2 → 5 Send R(ACK)0	Protocol error → 0		Send response S(WTX)	Protocol error → 0	Format error → 0	Transmission error n+1 N = n-1: Retry out → 0 N > n-1: Rule 5 → 6	Transmission error n+1 N = n-1: Retry out → 0 N > n-1: Rule 5 → 6
7: Receive wait state after sending R(NAK)0	Normal termination (n clear) → 0 Waiting for upper layer instructions	Block number violation → 0	Chaining continued (n clear) Rule 2 → 6 Send R(ACK)1	Block number violation → 0	Chaining continued (n clear) Rule 7 Send I(0)1 → 2 Send (1)1 → 4	Resend final I block (n clear) Rule 6 Send I(0)0 → 1 Send I(1)0 → 3				Transmission error n+1 N = n-1: Retry out → 0 N > n-1: Rule 4 → 7	Transmission error n+1 N = n-1: Retry out → 0 N > n-1: Rule 4 → 7
8: Receive wait state after sending R(NAK)1	Block number violation → 0	Normal termination (n clear) → 0 Waiting for upper layer instructions	Block number violation → 0	Chaining continued (n clear) Rule 2 → 5 Send R(ACK)0	Resend final I block (n clear) Rule 6 Send I(0)1 → 2 Send I(1)1 → 4	Chaining continued (n clear) Rule 7 Send I(0)0 → 1 Send I(1)0 → 3				Transmission error n+1 N = n-1: Retry out → 0 N > n-1: Rule 4 → 8	Transmission error n+1 N = n-1: Retry out → 0 N > n-1: Rule 4 → 8
9: Receive wait state after sending S(DESELECT) request	Rule 8 → 0										→ End of current protocol processing

Note 1: n: Error counter (initial value: 0), N: upper limit value of requests for resending

In the case event J or K occurs after requesting resending N times, the protocol ends and returns to status 0.



## 14. Card Test Methods

This section specifies the PICC test methods specified with ISO/IEC 10373-6, while also specifying the test method of PICC in consideration of the characteristics and so forth of the PCD as specified in these implementation specifications for the purpose of evaluating PICC.

In addition, compatibility verification equipment required for testing are also specified.

### 14.1 Test Environment

Unless specified otherwise, the test environment is to satisfy the conditions indicated in "Table 14.1-1 Test Environment".

Table 14.1-1 Test Environment

Item	Condition
Temperature	$23 \pm 3^{\circ}\text{C}(73^{\circ}\text{F} \pm 5^{\circ}\text{F})$
Humidity	Relative humidity of 40-60%

## 14.2 Test Apparatus

The test apparatus and test circuits for verifying the operation of PICC are specified. The following are included in the test apparatus.

(a) Compatibility Verification Equipment

- Calibration coil
- Test PCD
- Reference PICC

(b) Measuring Instrument

- Digital sampling oscilloscope

In addition, a test PCD-S having a small antenna shape of the PCD is specified as the compatibility verification equipment based on an assumption of a form of use based on these implementation specifications.

### 14.2.1 Calibration Coil

#### (1) Basic Specifications

##### (a) Size of the Calibration coil card

The calibration coil card shall consist of an area which has the height and width of an ID-a type defined in ISO/IEC 7810 containing a single turn coil concentric with the card outline.

An outline drawing of the calibration coil is shown in "Fig. 14.2-1 Calibration coil".

Outline according to ID1 of ISO/IEC 7810

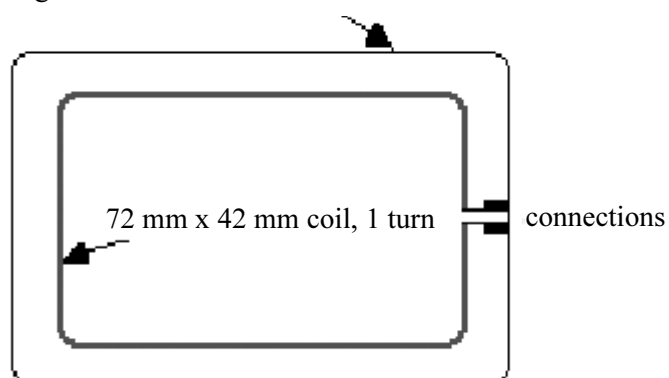


Fig. 14.2-1 Calibration coil

##### (b) Thickness and material of the Calibration coil card

The thickness of the calibration coil card shall be  $0.76 \text{ mm} \pm 10\%$ .

It shall be constructed of a suitable insulating material.

(c) Coil Characteristics

The coil on the calibration coil card shall have one turn.

The outer size of the coil shall be 72 mm x 42 mm with corner radius 5 mm. Relative dimensional tolerance shall be  $\pm 2\%$ .

(NOTE: The area over which the field is integrated is approximately 3000 mm<sup>2</sup>.)

The coil shall be made as a printed coil on PCB plated with 35  $\mu\text{m}$  copper. Track width shall be 500  $\mu\text{m}$  with a relative tolerance of  $\pm 20\%$ . The size of the connection pads shall be 1.5 mm x 1.5 mm.

(NOTE: At 13.56 MHz the approximate inductance is 200 nH, and approximate resistance is 0.25 Ohm.)

A high impedance oscilloscope probe (e.g.  $> 1\text{M}\Omega$ ,  $< 14\text{pF}$ ) shall be used to measure the (open circuit) voltage induced in the coil.

The resonance frequency of the calibration coil and connecting leads shall be above 60 MHz.

The open circuit calibration factor for this coil is 0,32 Volts (rms) per A/m (rms). [Equivalent to 900 mV (peak-to-peak) per A/m (rms)]

(NOTE: The signal on the terminals of the calibration coil should be measured with high impedance probe which does not load the coil significantly.)

## (2) Extended Specifications

Two types of calibration coils consisting of calibration coil S and calibration coil L having different coil surface areas than the calibration coil specified in the basic specifications are specified in order to consider magnetic field distribution.

### (a) Calibration Coil Dimensions

An outline drawing of the calibration coil is shown in "Fig. 14.2-2 Calibration coil".

The calibration coil S card and calibration coil L card shall consist of an area which has the height and width defined in ISO/IEC 7810 containing a single turn coil concentric with the card outline.

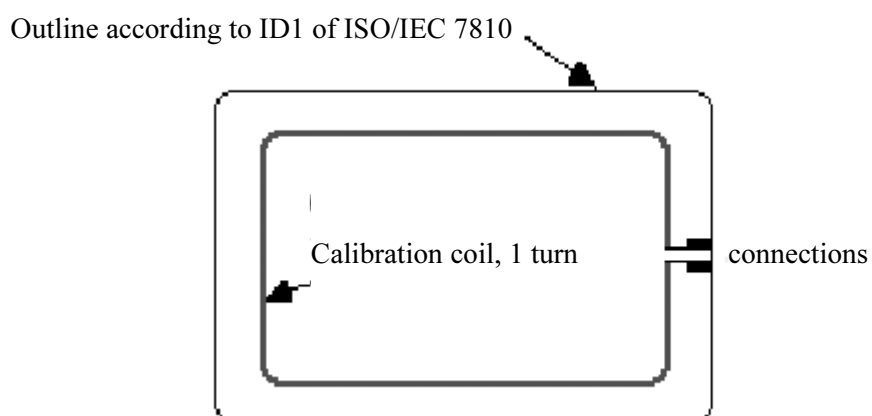


Fig. 14.2-2 Calibration coil

### (b) Thickness and material of the Calibration coil card

The thickness of the calibration coil card shall be  $0.76 \text{ mm} \pm 10\%$ .

It shall be constructed of a suitable insulating material.

## (c) Coil Characteristics

Calibration coil characteristics are shown in "Table 14.2-1 Calibration Coil Characteristics".

Table 14.2-1 Calibration Coil Characteristics

Item	Description		
	Calibration coil - S	Calibration coil - L	Calibration coil (basic specifications)
Coil dimensions	66.6 mm $\pm$ 2% x 31 mm $\pm$ 2%, corner R 8.5 mm $\pm$ 2%	83.6 mm $\pm$ 2% x 52 mm $\pm$ 2%, corner R 5 mm $\pm$ 2%	72 mm $\pm$ 2% x 42 mm $\pm$ 2%, corner R 5 mm $\pm$ 2%
Coil area	2003 mm <sup>2</sup>	4326 mm <sup>2</sup>	3003 mm <sup>2</sup>
Conversion to magnetic field	1 A/m (rmS) = 214.4 mV (rmS)	1 A/m (rmS) = 463. 1mV (rmS)	1 A/m (rmS) = 320 mV (rmS)
Pattern width	0.5 mm $\pm$ 20%	Same as left	Same as left
Pattern interval	0.5 mm $\pm$ 20%	Same as left	Same as left
Pattern material	Copper foil	Same as left	Same as left
Pattern thickness	35 $\mu$ m	Same as left	Same as left
No. of turns	1 turn	Same as left	Same as left
Inductance (at 13.56 MHz)	-	-	200 nH
Resistance value (at 13.56 MHz)	-	-	0.25 Ohm

## (3) References

None

## 14.2.2 Test PCD

### (1) Basic Specifications

The test PCD assembly shall consist of a 150mm diameter PCD antenna and two parallel sense coils: sense coil a and sense coil b. The test set-up is shown in "Fig. 14.2-3 Load Modulation Measuring Circuit". The sense coils shall be connected such that the signal from one coil is in opposite phase to the other. The 50 Ohm potentiometer serves to fine adjust the balance point when the sense coils are not loaded by a PICC or any magnetically coupled circuit. The capacitive load of the probe including its parasitic capacitance shall be less than 14 pF.

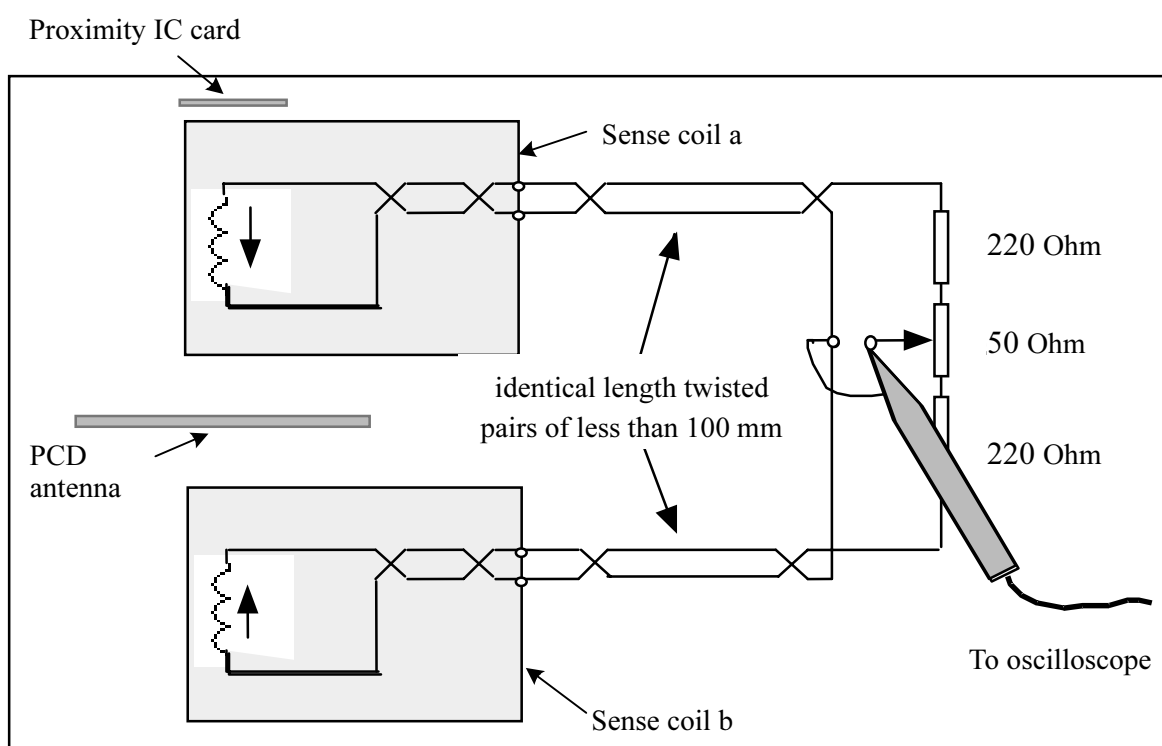


Fig. 14.2-3 Load Modulation Measuring Circuit

## (a) Test PCD Antenna

The Test PCD antenna shall have a diameter of 150 mm and its construction shall conform to the drawings in "(d) Test PCD Antenna".

The tuning of the antenna may be accomplished with the procedure given in "(e) Test PCD Antenna Adjustment".

## (b) Sense Coils

The size of the sense coils shall be 100 mm x 70 mm. The sense coil construction shall conform to the drawings in "(f) Sensor Coils".

## (c) Assembly of Test PCD

The sense coils and Test PCD antenna shall be assembled parallel and with the sense and antenna coils coaxial and such that the distance between the active conductors is 37.5mm as in "Fig. 14.2-4 Test PCD Assembly".

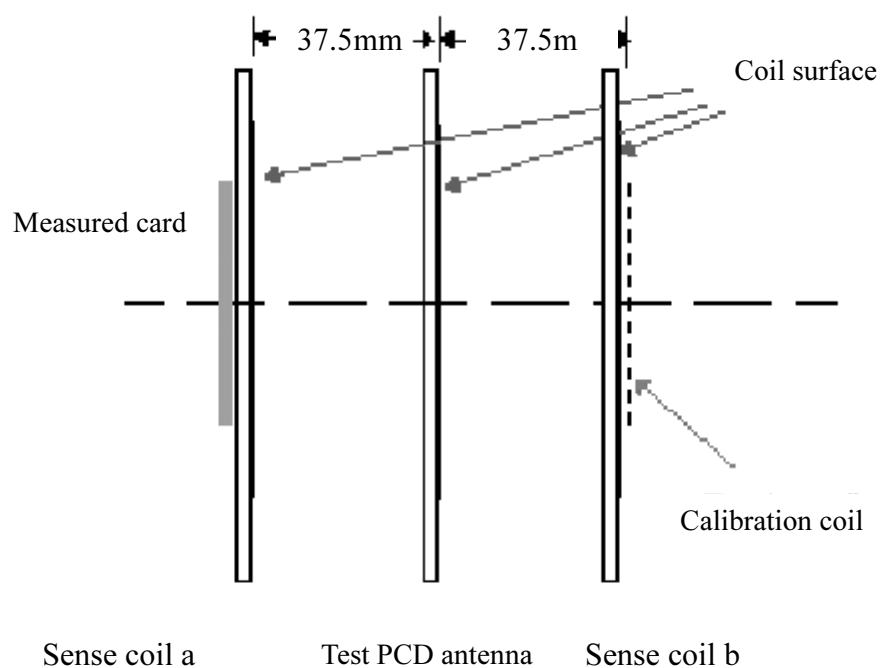


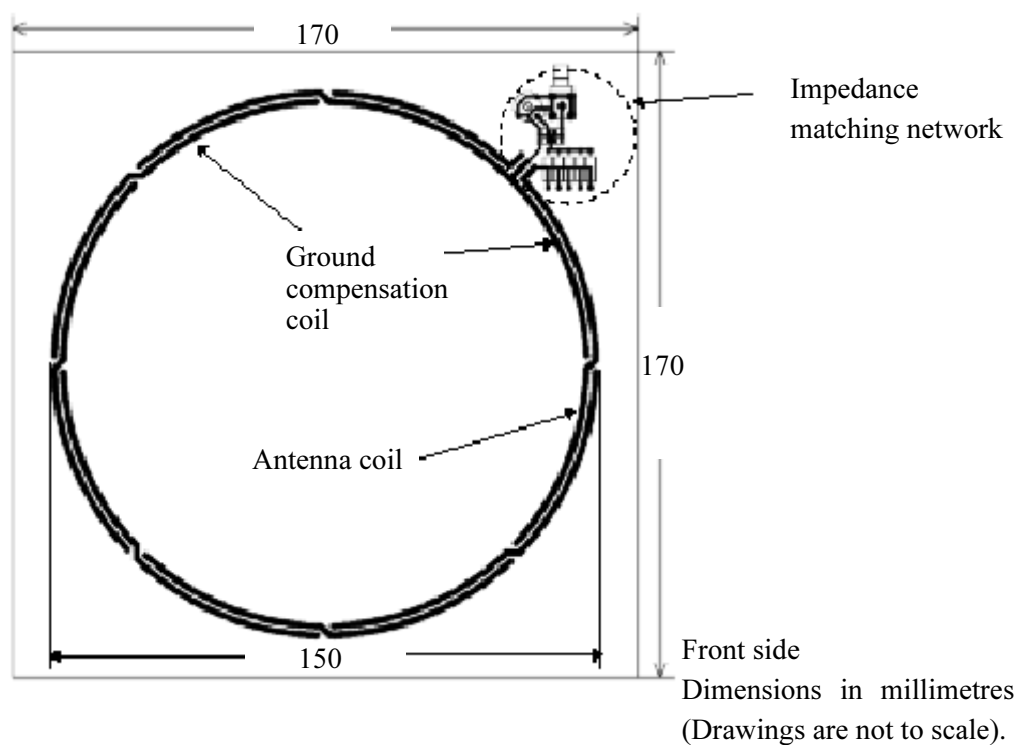
Fig. 14.2-4 Test PCD Assembly



## (d) Test PCD Antenna

## a) Layout Drawing of Antenna and Impedance Matching Network

The structure of the test PCD antenna is shown in "Fig. 14.2-5 Test PCD Antenna Layout (View from front)" and "Fig. 14.2-6 Test PCD Antenna Layout (View from back)".



(Note: The antenna coil track width is 1.8 mm (except for through-plated holes).  
Starting from the impedance matching network there are crossovers every 45°.  
PCB: FR4 material thickness 1.6 mm, double sided with 35  $\mu\text{m}$  copper.)

Fig. 14.2-5 Test PCD Antenna Layout (View from front)



Back side

Fig. 14.2-6 Test PCD Antenna Layout (View from back)

b) Impedance matching network

The antenna impedance ( $R_{ant}$ ,  $L_{ant}$ ) is adapted to the signal generator output impedance ( $Z=50\text{ Ohm}$ ) by a matching circuit (see "Fig. 14.2-7 Impedance Matching Network" and "Table 14.2-2 Component Table").

The capacitors  $C_1$ ,  $C_2$  and  $C_3$  have fixed values. The input impedance phase can be adjusted with the variable capacitor  $C_4$ .

(Note: Care has to be taken to keep maximum voltages and maximum power dissipation within the specified limits of the individual components.)

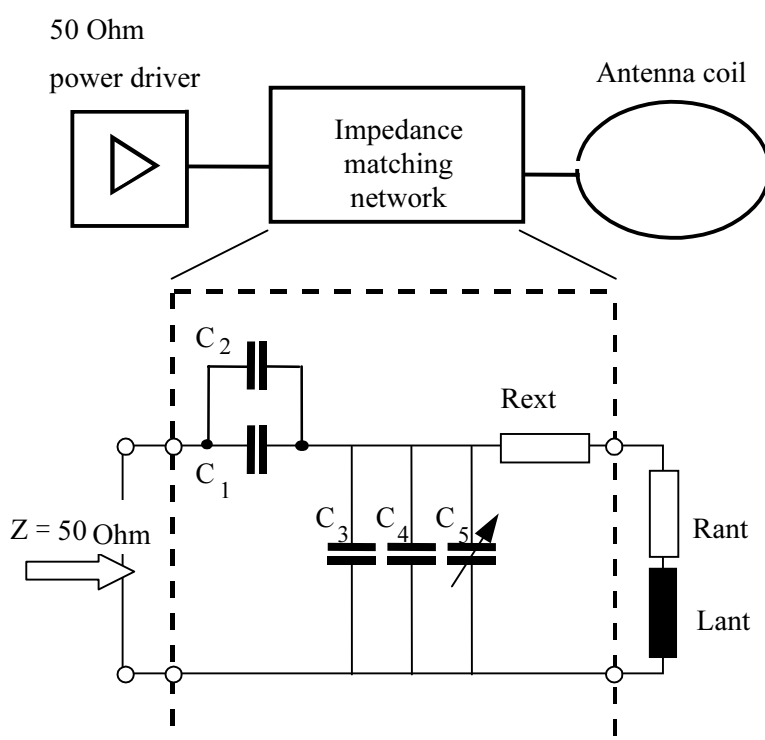


Fig. 14.2-7 Impedance Matching Network

Table 14.2-2 Component Table

	Value	Unit
$C_1$	39	pF
$C_2$	8.2	pF
$C_3$	180	pF
$C_4$	33	pF
$C_5$	2 - 27	pF
$R_{ext}$	5 x 4.7 (parallel)	Ohm

## (e) Test PCD Antenna tuning

A two step simple phase tuning procedure is used to match the impedance of the antenna to that of the driving generator. After the two steps of the tuning procedure the signal generator shall be directly connected to the antenna output for the tests.

## Step 1:

A high precision resistor of  $50\ \Omega \pm 1\%$  (e.g. 50 Ohm BNC resistor) is inserted in the signal line between the signal generator output and an antenna connector. The two probes of the oscilloscope are connected to both sides of the serial reference resistor. The oscilloscope displays a Lissajous figure when it is set in Y to X presentation.

The signal generator is set to:

Wave form: Sinusoidal

Frequency: 13.56 MHz

Amplitude: 2V (rms) - 5V (rms)

The probe, which is in parallel to the output connector has a small parasitic capacitance  $C_{\text{probe}}$ . A calibration capacitance  $C_{\text{cal}}$  in parallel to the output connector compensates this probe capacitor if  $C_{\text{cal}} = C_{\text{probe}}$ . The output is terminated with a second high precision resistor of  $50\ \Omega \pm 1\%$  (e.g. 50 Ohm BNC terminating resistor). The probe capacitor is compensated when the Lissajous figure is completely closed.

The adjustment method is shown in "Fig. 14.2-8 Calibration set-up - Step1".

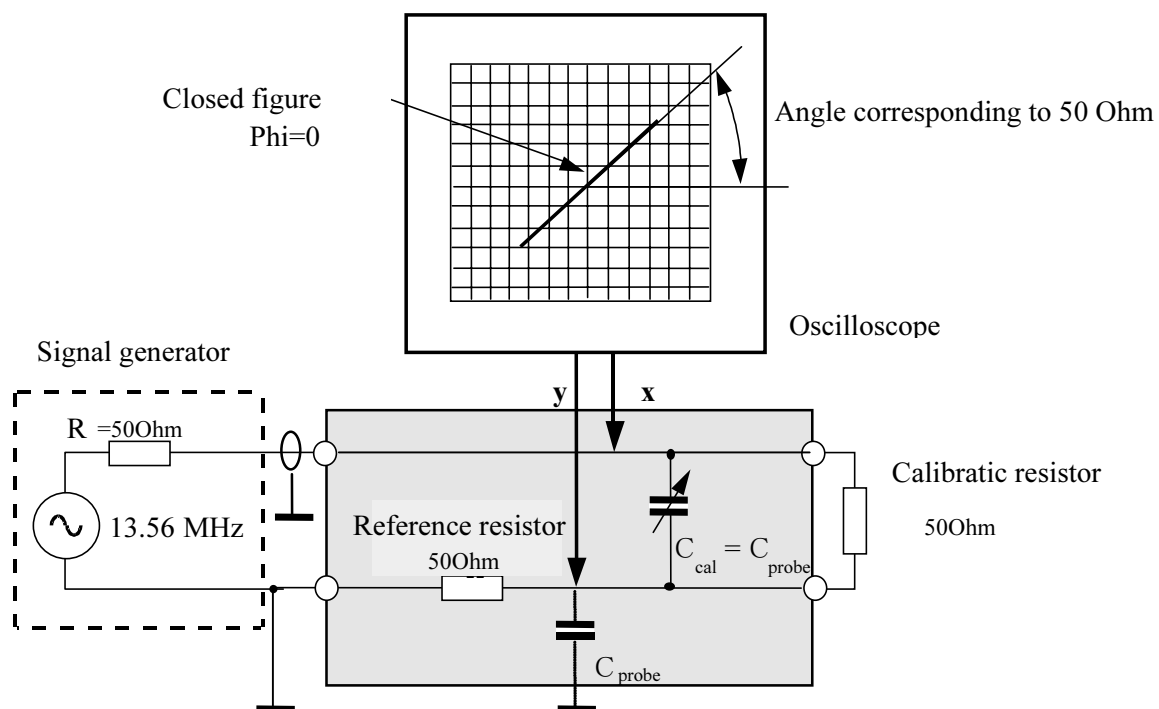


Fig. 14.2-8 Calibration set-up - Step 1

(Note: The ground cable has to be run close to the probe to avoid induced voltages caused by the magnetic field.)

**Step 2:**

Using the same values as set for step 1, in the second step the matching circuitry is connected to the antenna output. The capacitor  $C_5$  on the antenna board is used to tune the phase to zero. The adjustment method is shown in "Fig. 14.2-9 Calibration set-up - Step 2".

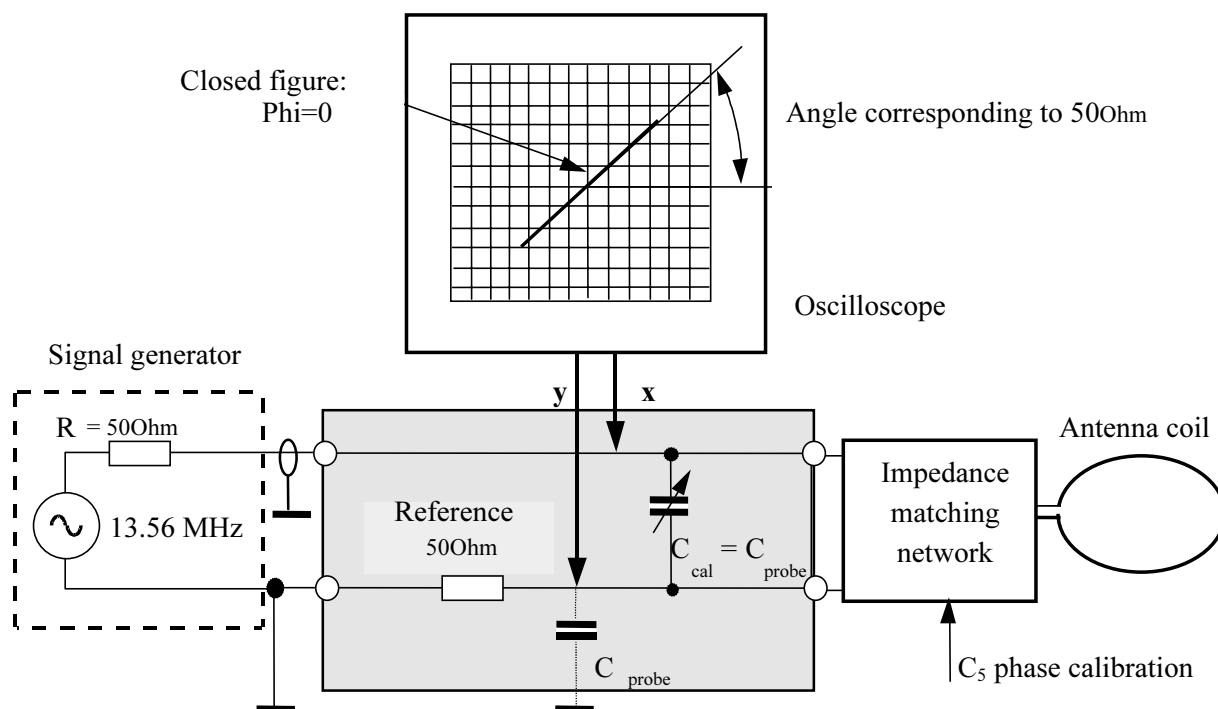
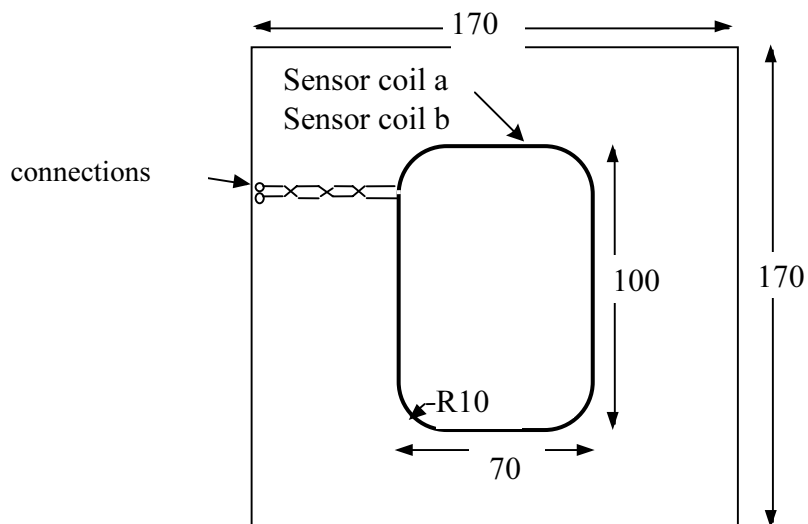


Fig. 14.2-9 Calibration set-up - Step 2

## (f) Sense Coils

## a) Sense coil layout

The structure of the sensor coil is shown in "Fig. 14.2-10 Sense Coil Layout".



Dimensions in millimetres  
(Drawings are not to scale).

(Note: PCB: FR4 material thickness 1.6 mm, double sided with 35  $\mu$ m copper.) The sense coil track width is 0.5 mm with relative tolerance  $\pm 20\%$  (except for through-plated holes). Size of the coils refers to the outer dimensions.

Fig. 14.2-10 Sense Coil Layout

## b) Sense Coil Assembly

The sensor coil assembly drawing is shown in "Fig. 14.2-11 Sense Coil Assembly". This assembled state is the test PCD.

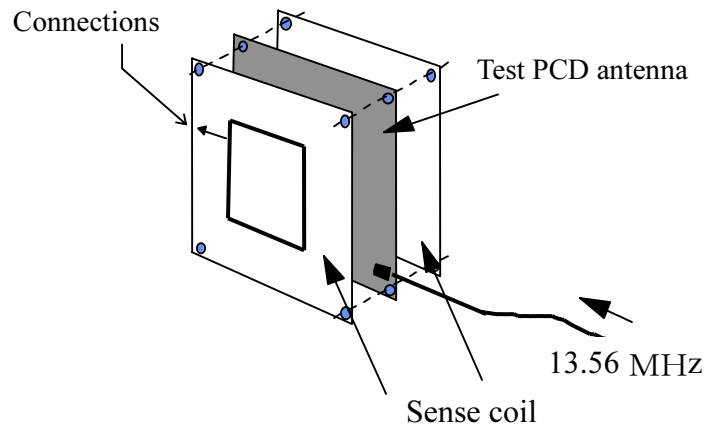


Fig. 14.2-11 Sense Coil Assembly



(2) Extended Specifications

a) Impedance Matching Network

The impedance matching network is shown in "Fig. 14.2-12 Impedance Matching Network" and "Table 14.2-3 Component Table".

This network has adjustment capacitor C6 added to the basic specifications, and is used to more accurately perform impedance adjustment.

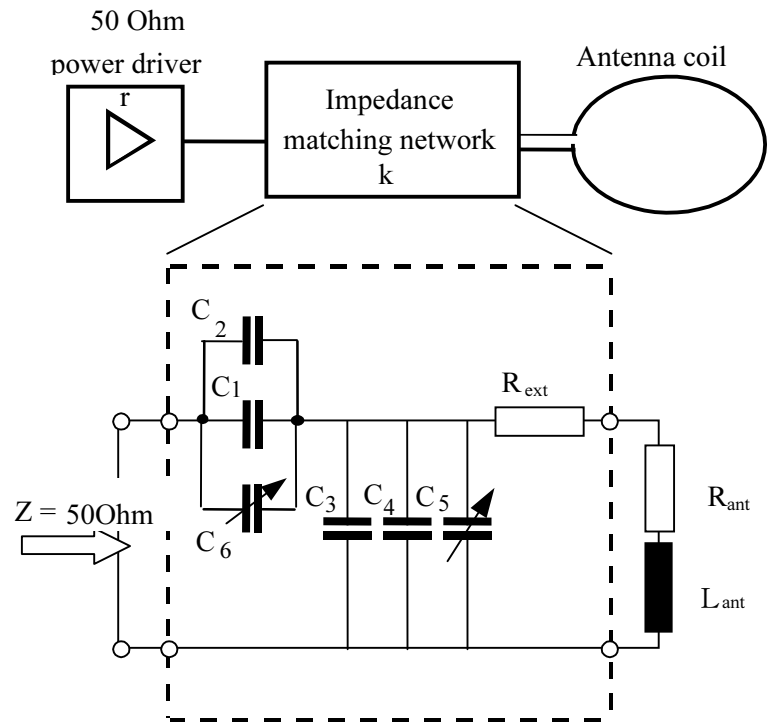


Fig. 14.2-12 Impedance Matching Network

Table 14.2-3 Component Table

	Value	Unit
C1	39	pF
C2	8.2	pF
C3	180	pF
C4	33	pF
C5	2 - 27	pF
C6	2 - 27	pF
R <sub>ext</sub>	5 x 4.7 (parallel)	Ohm

b) Test PCD Antenna tuning

1) Adjustment Using an Oscilloscope

Phase adjustment is performed with capacitors C5 and C6 in step 2 for the adjustment method specified in the basic specifications.

2) Adjustment Using Network Analyzer

The test PCD is connected to a network analyzer followed by measurement of impedance by measuring S11. Adjustment is made so that the impedance of the test PCD antenna reaches an impedance of  $50\ \Omega \pm 1\%$  (induction component or capacitance component shall be 0  $\Omega$ ) at a frequency of 13.56 MHz.

(3) References

None

### 14.2.3 Test PCD-S

#### (1) Basic Specifications

None

#### (2) Extended Specifications

##### (a) Test PCD-S Antenna

Antenna specifications of the test PCD-S are shown in "Table 14.2-4 Test PCD-S Antenna Specifications".

Table 14.2-4 Test PCD-S Antenna Specifications

Name	Description	
Antenna coil	Coil outer diameter	$\phi 38 \pm 0.2\text{mm}$
	Pattern width	0.5mm
	Pattern interval	0.5mm
	Pattern thickness	35 $\mu\text{m}$
	No. of turns	3 turns
	Structure	Formed with copper foil on a printed board
Antenna board	Size	120mm $\times$ 100mm
	Thickness	t1.6mm
	Material	FR4
Impedance matching network	Impedance is matched between the antenna coil and output circuit at 50 Ohm.	

##### (b) Structure

The test PCD-S circuit is shown in "Fig. 14.2-13 Test PCD-S Circuit ", while the structure of the test PCD-S is shown in "Fig.14.2-14 Test PCD-S Structure".

The calibration coil and test PCD-S antenna shall be arranged in parallel so that the central axes of the calibration coil and test PCD-S antenna coil are aligned. At this time, the test PCD-S is assembled so that the interval between the effective conductor surfaces is 15 mm as shown in "Fig. 14.2-14 Test PCD-S Structure".

In addition, a 5 mm spacer is arranged between the test PCD-S and measured card, and the spacer surface is defined as the reference surface (distance: 0 mm) of the test PCD-S, while the antenna center of the test PCD-S is defined as the central position.

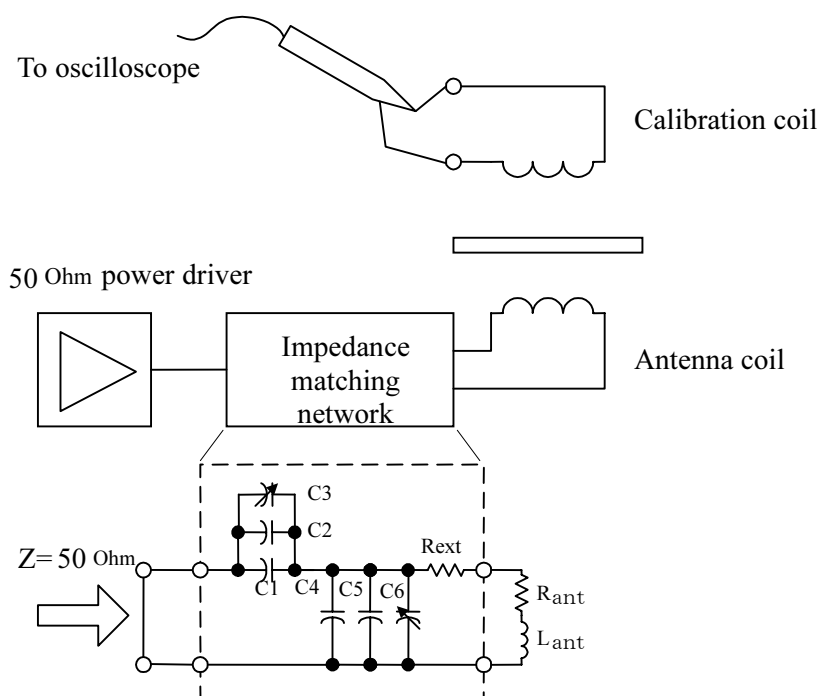


Fig. 14.2-13 Test PCD-S Circuit

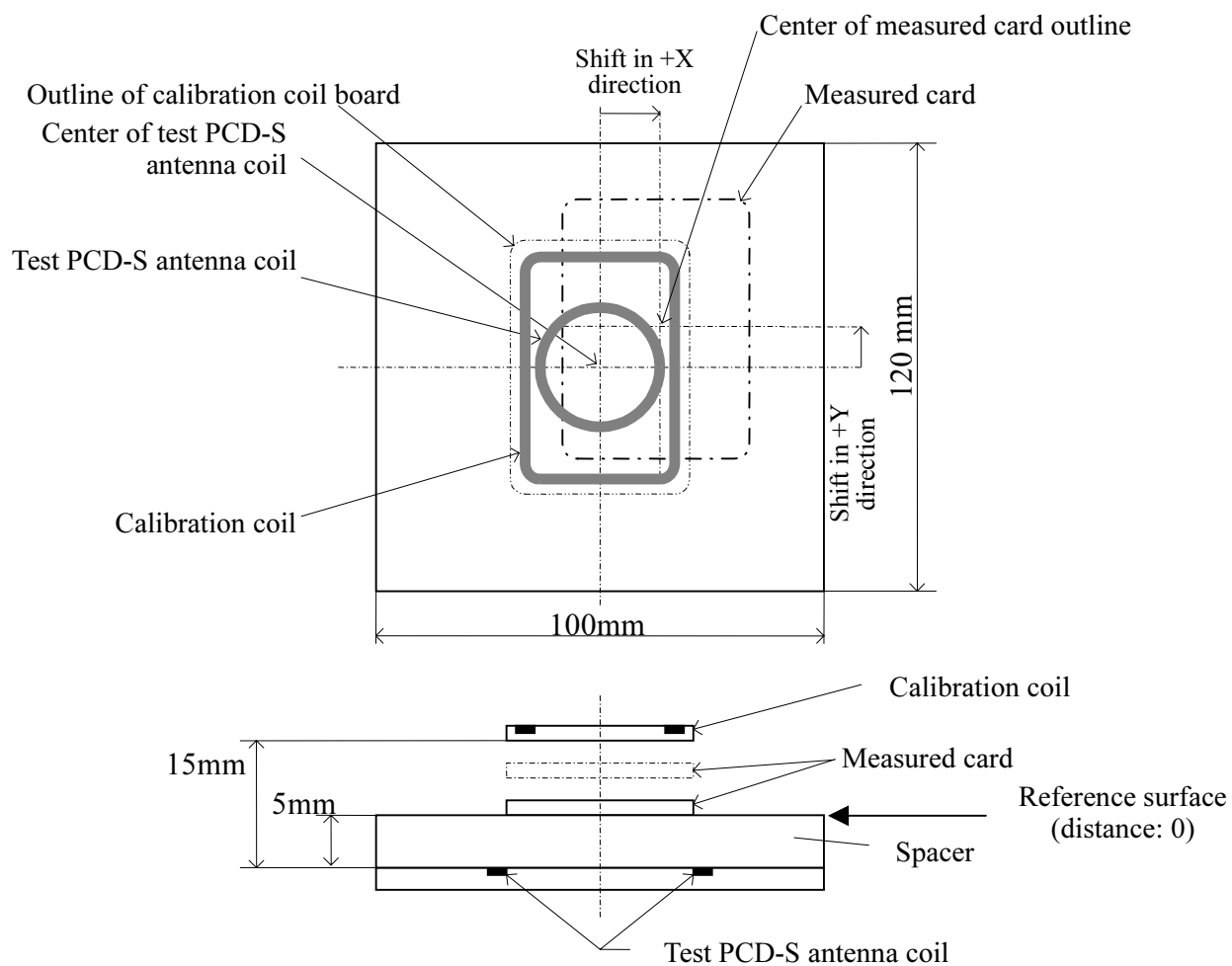


Fig. 14.2-14 Test PCD-S Structure

## c) Calibration

## a) Antenna Output

The antenna output is to be magnetic field strength (7) A/m  $\pm 5\%$  at the calibration coil. The position of the calibration coil is to be at distance 0 mm without any shift.

## b) Modulation Waveform

The modulation waveform is calibrated so that the modulation waveform becomes the specified waveform by measuring the modulation waveform at the calibration coil. The position of the calibration coil is to be at distance 0 mm without any shift.

## (3) References

None

#### 14.2.4 Digital Sampling Oscilloscope

##### (1) Basic Specifications

The digital sampling oscilloscope shall be capable of sampling at a rate of at least 100 million samples per second with a resolution of at least 8 bits at optimum scaling. The oscilloscope should have the capability to output the sampled data as a text file to facilitate mathematical and other operations such as windowing on the sampled data using external software programs.

##### (2) Extended Specifications

None

##### (3) References

None

## 14.3 Test Methods

### 14.3.1 Testing Using Test PCD

#### 14.3.1.1 Functional Tests

##### (1) Basic Specifications

This test measures the amplitude of the load modulation signal of the PICC within the operating magnetic field region defined by the PCD.

##### (a) Test Method

###### Step 1:

The load modulation test circuit shown in "Fig. 14.2-3 Load Modulation Measuring Circuit" and the test PCD shown in "Fig. 14.2-4 Test PCD Assembly" are used.

Adjust the current in the PCD antenna to the required field strength as measured by the calibration coil. Connect the output of the load modulation test circuit of "Fig 14.2-3 Load Modulation Measuring Circuit" to the digitizing sampling oscilloscope. The 50 Ohm potentiometer shall be trimmed to minimize the residual carrier. This signal shall be at least 40dB lower than the signal obtained by shorting one sense coil.

(Note: The waveform of the load modulated subcarrier ( $f_c$ ) is measured with a digitizing sampling oscilloscope capable of sampling at a rate of 100 million samples per second with a resolution of 8 bits at optimum scale.)

###### Step 2:

The PICC under test shall be placed in the DUT position, concentric with sense coil a. The RF drive into the test PCD antenna shall be re-adjusted to the required field strength.

Display a segment of at least two cycles of the waveform of the subcarrier load modulation on the digital sampling oscilloscope and store the sampled data in a file for analysis by a computer software programme.

Fourier transform exactly two subcarrier cycles of the sampled modulation waveform using suitable computer software. Use a discrete Fourier transformation with a scaling such that a pure sinusoidal signal results in its peak magnitude. To minimize transient effects, avoid a subcarrier cycle immediately following a non-modulation period.

The resulting peak amplitudes of the upper and lower sidebands at  $f_c + f_s$  and  $f_c - f_s$  shall be above the value defined in "10.1.2 Load Modulation".

A REQA or a REQB command sequence as define in "12. Anticollision" shall be sent by the Test PCD to obtain a signal or load modulation response from the PICC.



## (b) Measurements

The amplitude values of the upper and lower band frequencies of  $(f_C + f_S)$  and  $(f_C - f_S)$  of the response signal generated by the PICC are measured.

## (2) Extended Specifications

These test items only apply to cards premised on two card operation.

## (a) Test Method

Testing is performed under the condition of superimposing two card to be tested.

## a) Case of Superimposing Two PICC

Place two PICC in the test PCD while superimposing them on each other after which an REQ signal is sent by the test PCD. Check the modulation signal from the PICC with an oscilloscope connected to the calibration coil. In the case the response from the two PICC interferes, perform anticollision processing and measure in the absence of collision.

## b) Case of Superimposing a PICC and Reference PICC

Place the PICC in the test PCD while superimposed with the power transmission testing reference PICC (3 types) as specified in "15.2.1 Reference PICC" after which an REQ signal is sent by the test PCD. Check the modulation signal from the PICC with an oscilloscope connected to the calibration coil.

## (b) Measurements

Measure the amplitude values of the upper and lower band frequencies  $(f_C + f_S)$  and  $(f_C - f_S)$  of the response signal generated by the PICC.

## (3) References

None

### 14.3.1.2 Minimum Operating Magnetic Field Test

This test measures the minimum operating magnetic field of the PICC.

#### (1) Basic Specifications

##### (a) Test Method

The minimum operating magnetic field at which a response is generated from the PICC is measured according to the test method specified in the extended specifications of "14.3.1.1 Functional Tests".

##### (b) Specifications

The minimum operating magnetic field must satisfy "8.2 Operating Magnetic Field".

#### (2) Extended Specifications

These test items apply only to cards premised on two card operation.

##### (a) Test Method

The minimum operating magnetic field at which a response is generated from the PICC is measured according to the test method specified in the basic specifications of "14.3.1.1 Functional Tests".

##### (b) Specifications

The minimum operating magnetic field must satisfy "8.2 Operating Magnetic Field".

#### (3) References

None

### 14.3.1.3 Maximum Operating Magnetic Field Test

This test measures the maximum operating magnetic field of the PICC.

#### (1) Basic Specifications

##### (a) Test Method

The maximum operating magnetic field at which a response is generated from the PICC is measured according to the test method specified in the extended specifications of "14.3.1.1 Functional Tests".

##### (b) Specifications

The maximum operating magnetic field must satisfy "8.2 Operating Magnetic Field".

#### (2) Extended Specifications

These test items apply only to cards premised on two card operation.

##### (a) Test Method

The maximum operating magnetic field at which a response is generated from the PICC is measured according to the test method specified in the basic specifications of "14.3.1.1 Functional Tests".

##### (b) Specifications

The maximum operating magnetic field must satisfy "8.2 Operating Magnetic Field".

#### (3) References

None

#### 14.3.1.4 Maximum Applied Magnetic Field Test

This test measures the maximum applied magnetic field of the PICC.

##### (1) Basic Specifications

None

##### (2) Extended Specifications

##### (a) Test Method

###### a) Case of a Single Card

Attach a single PICC at the location of the measured card of the test PCD and apply the maximum applied magnetic field as specified in "8.2 Operating Magnetic Field".

After applying the magnetic field, check the function of the PICC according to the test method specified in the basic specifications of "14.3.1.1 Functional Tests".

###### b) Case of Superimposing Two Cards

These test items apply only to cards premised on two card operation.

###### 1) Case of Superimposing Two PICC

Attach the two PICC at the location of the measured card of the test PCD while superimposed on each other, and apply the maximum applied magnetic field specified in "8.2 Operating Magnetic Field".

After applying the magnetic field, check the function of the PICC according to the test method specified in the basic specifications of "14.3.1.1 Functional Tests".

###### 2) Case of Superimposing a PICC and Reference PICC

Attach the PICC at the location of the measured card of the test PCD while superimposed with a single power transmission testing reference PICC as specified in "15.2.1 Reference PICC", and apply the maximum applied magnetic field specified in "8.2 Operating Magnetic Field".

After applying the magnetic field, check the function of the PICC according to the test method specified in the basic specifications of "14.3.1.1 Functional Tests".

##### (b) Specifications

The PICC must function normally after applying the magnetic field.

##### (3) References

None

### 14.3.1.5 Signal Receive Test

This tests the signal receive function of the PICC.

#### (1) Basic Specifications

None

#### (2) Extended Specifications

##### (a) Test Method

The modulation signal from the test PCD is adjusted to the modulation waveform specified in "9.1.2 Modulation" or "9.2.2 Modulation".

Measure the response from the PICC according to the test method specified in the basic specifications of "14.3.1.1 Functional Tests".

##### (b) Specifications

The response from the PICC must be generated in the form of the modulation waveform specified in "9.1.2 Modulation" or "9.2.2 Modulation" within the range specified in "8.2 Operating Magnetic Field".

#### (3) References

None

#### 14.3.1.6 Load Modulation Test

This test measures the magnitude of the load modulation of the PICC.

##### (1) Basic Specifications

###### (a) Test Method

Measure the response from the PICC according to the test method specified in the basic specifications of "14.3.1.1 Functional Tests".

###### (b) Specifications

The PICC must satisfy the specifications of "10.1.2 Load Modulation" or "10.2.2 Load Modulation".

##### (2) Extended Specifications

These test items apply only to cards premised on two card operation.

###### (a) Test Method

Measure the response from the PICC according to the test method specified in the extended specifications of "14.3.1.1 Functional Tests".

###### (b) Specifications

The PICC must satisfy the specifications of "10.1.2 Load Modulation" or "10.2.2 Load Modulation".

##### (3) References

None

### 14.3.1.7 Reference PICC Superimposition Test

#### (1) Basic Specifications

None

#### (2) Extended Specifications

These test items apply only to cards premised on two card operation.

The effect of the PICC on the reference PICC specified in "15.2.1 Reference PICC" is measured.

#### (a) Power Transfer Testing

##### a) Testing Using Test PCD

##### 1) Test Method

Connect jumper J1 to resistor R3 of the power transmission testing reference PICC specified in the extended specifications of "15.2.1 Reference PICC", attach two superimposed power transmission testing reference PICC at the position of the measured card of the test PCD, and adjust the output of the test PCD so that the voltage at both ends of R3 of the power transmission testing reference PICC becomes 6.8 V.

Next, attach a PICC superimposed with a single power transmission testing reference PICC at the location of the measured card of the test PCD, and measure the received power of the power transmission testing reference PICC .

##### b) Specifications

The received voltage of the reference PICC must be 6.8 V or more.

#### (3) References

None

## 14.3.2 Testing Using Test PCD-S

### 14.3.2.1 Functional Tests

#### (1) Basic Specifications

None

#### (2) Extended Specifications

None

#### (3) References

Confirm that the PICC operates with the test PCD-S.

#### (a) Test Method

Place the measured card in the test PCD-S and send REQA or REQB as specified in "12. Anticollision" from the test PCD-S. Check the modulation signal from the PICC with an oscilloscope connected to the calibration coil.

Perform testing for both the case of using a single card and superimposing two cards. When superimposing two cards, measure for two superimposed measured cards as well as for the case of superimposing the measured card with the power transmission testing reference PICC specified in "15.2.1 Reference PICC".

#### (b) Measurements

Check the modulation signal from the PICC over the operating range of the test PCD-S.

- Test PCD-S operating range:

Distance: 0-5 mm

Shift: ø 5 mm

#### (c) Specifications

There must be a modulation signal from the PICC over the operating range of the test PCD-S.



## 15. PCD Test Methods

In addition to specifying test methods of the PCD based on ISO/IEC 10373-6, test methods of the PCD are specified in consideration of PICC characteristics specified in these implementation specifications for the purpose of evaluating the PCD.

In addition, compatibility verification equipment required for testing are also specified.

### 15.1 Test Environment

Unless specified otherwise, the test environment is to satisfy the conditions indicated in "Table 15.1-1 Test Environment".

Table 15.1-1 Test Environment

Item	Condition
Temperature	$23 \pm 3^{\circ}\text{C}$ ( $73^{\circ}\text{F} \pm 5^{\circ}\text{F}$ )
Humidity	Relative humidity of 40-60%

## 15.2 Test Apparatus

The test apparatus and test circuits for verifying the operation of PCD are specified based on ISO/IEC 10373-6. The test apparatus include that indicated below.

- (a) Compatibility Verification Equipment
  - Reference PICC

### 15.2.1 Reference PICC

The reference PICC used to evaluate the performance of PCD is specified.

#### (1) Basic Specifications

Reference PICCs are defined:

- to test  $H_{\min}$  and  $H_{\max}$  produced by a PCD (under conditions of loading by a PICC)
- to test the ability of a PCD to power a PICC
- to detect the minimum load modulation signal from the PICC.

#### (a) Reference PICC for Power Transmission Testing

This is used for measurement of the minimum and maximum generated magnetic fields as well as power transmission testing.

The schematic for the power transmission test is shown in "15.2.1 (f) a) Reference PICC for Power Transmission Testing". Resistors R1 and R2 may be selected by means of jumper J1. The resonant frequency can be adjusted with capacitor CV1.

#### (b) Reference PICC for Load Modulation Testing

The schematic for load modulation testing is shown in "15.2.1 (f) b) Reference PICC for Load Modulation Testing". The load modulation can be chosen to be resistive or capacitive.

This reference PICC is calibrated by using the Test PCD assembly as follows:

- Place reference PICC in the position of the DUT.
- Measure the load modulation signal amplitude as described in "14.3.1.1 Functional Tests". This amplitude should correspond to the minimum amplitude at values of field strength required by "10.1.2 Load Modulation".

(c) Dimensions of the Reference PICCs

The Reference PICCs shall consist of an area containing the coils which has the height and width defined in ISO/IEC 7810 for ID-1 type. An area external to this, containing the circuitry which emulates the required PICC functions, shall be appended in such a way as to allow insertion into the test set-ups described below and so as to cause no interference to the tests. The dimensions shall be as in "Fig. 15.2-1 Reference PICC Dimensions".

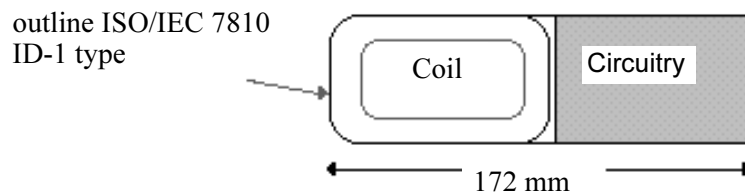


Fig. 15.2-1 Reference PICC Dimensions

(d) Thickness of the Reference PICCs board

The thickness of the Reference PICCs active area shall be  $0.76 \text{ mm} \pm 10 \%$ .

(e) Coil Characteristics

The coil in the active area of the Reference PICCs shall have 4 turns and shall be concentric with the area outline.

The outer size of the coils shall be  $72 \text{ mm} \times 42 \text{ mm}$  with a relative tolerance of  $\pm 2 \%$ .

The coil shall be printed on PCB plated with  $35 \text{ }\mu\text{m}$ .

Track width and spacing shall be  $500 \text{ }\mu\text{m}$  with a relative tolerance of  $\pm 20 \%$ .

(f) Circuit Drawing

a) Reference PICC for Power Transmission Testing

The circuit drawing of the power transmission testing reference PICC is shown in "Fig. 15.2-2 Schematic of Power Transmission Testing Reference PICC ", while the components list is shown in "Table 15.2-1 Components List".

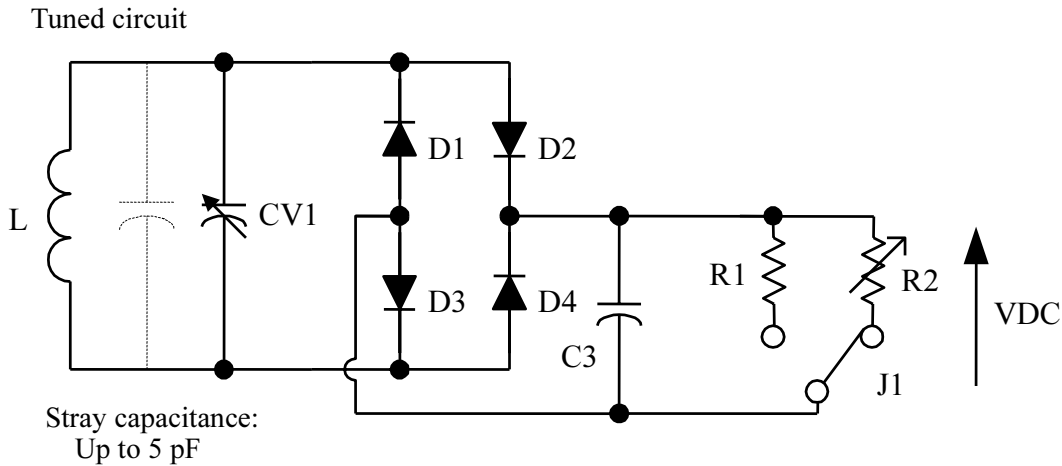


Fig. 15.2-2 Schematic of Power Transmission Testing Reference PICC

Table 15.2-1 Components List

Component	Specifications
L (Coil)	See (e) Coil Characteristics
CV1	6-60pF
C3	10nf
D1, D2, D3, D4	See Table 15.2-2 (BAR43 or equivalent)
R1	1.8 kOhm (5 mW)
R2	0-5kOhm

Table 15.2-2 Basic Characteristics of Diodes D1, D2, D3 and D4

Item	Test conditions (T <sub>j</sub> = 25°C)	Typical	Max. value	Units
V <sub>r</sub>	I <sub>r</sub> =2mA		0.33	V
C	V <sub>R</sub> =1V F=1MHz	7		pF
t <sub>rr</sub>	I <sub>F</sub> =10mA, I <sub>R</sub> =1mA, I <sub>rr</sub> =1mA		5	ns

V<sub>F</sub> Forward voltage drop  
V<sub>R</sub> Reverse voltage  
I<sub>F</sub> Forward current  
I<sub>R</sub> Reverse current  
t<sub>rr</sub> Recovery time  
I<sub>rr</sub> Recovery current  
T<sub>j</sub> Junction temperature  
F Frequency  
C Junction capacitance

## b) Reference PICC for Load Modulation Testing

The schematic for the reference PICC for load modulation testing is shown in "Fig. 15.2-3 Schematic of Reference PICC for Load Modulation Testing", the components for adjusting characteristics are shown in "Table 15-2-3 Emulation Circuit Adjustable Component List", and fixed components are shown in "Table 15-2-4 Components List".

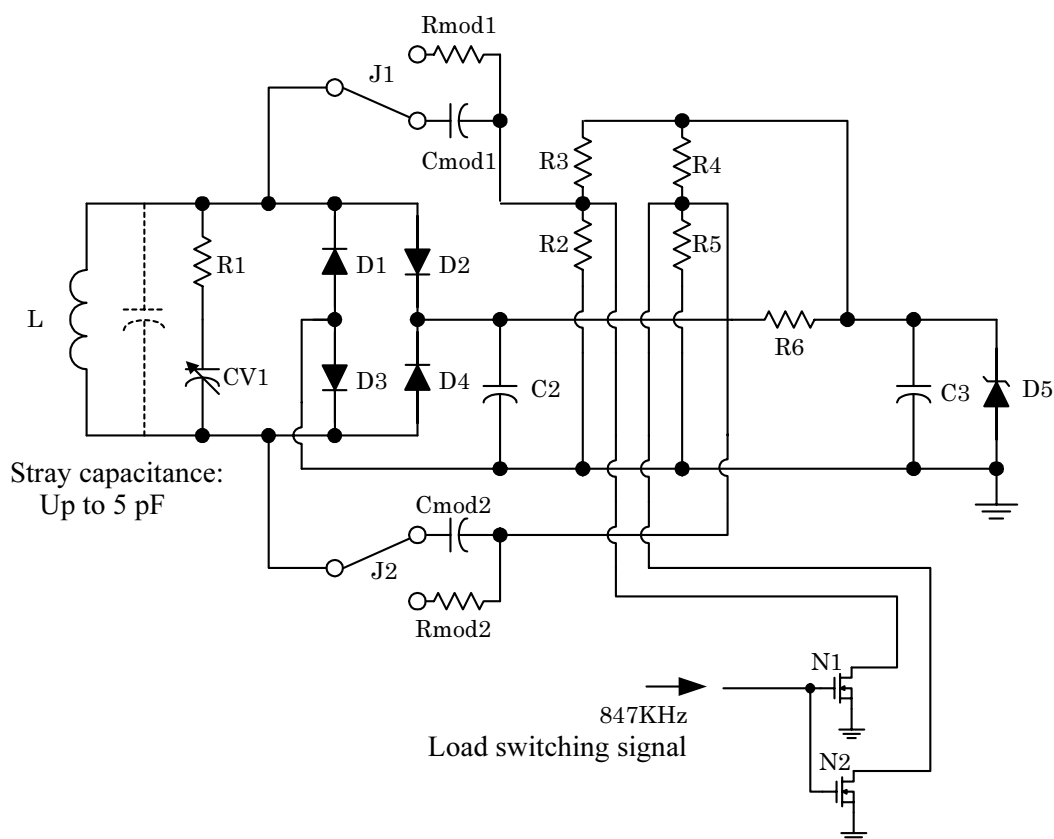


Fig. 15.2-3 Schematic of Reference PICC for Load Modulation Testing

Table 15-2-3 Emulation Circuit Adjustable Component List

Component	Function	Specifications
R1	adjust Q	0~10 Ohm
CV1	adjust resonance	Accordig to a request
Cmod1, Cmod2	Capacitive modulation	3.3~10 pF
Rmod1, Rmod2	Resistive modulation	400~12 kOhm
R6	Shunt Current	10 Ohm~5 kOhm
D5	Shunt Voltage	2.7~15 V

Table 15-2-4 Components List

Component	Specifications
R2	1 MOhm
R3	1 MOhm
R4	1 MOhm
R5	1 MOhm
D1, D2, D3, D4	See Table 15.2-2 (BAR43 or equivalent)
L (Coil)	See (e) Coil Characteristics
CV1	6-60 pF
C2	100 pF
C3	10 nf
N1, N2	N-MOS transistor (ground capacitance of 10 pF or less)

## (2) Extended Specifications

A reference PICC having a different coil shape and circuit constant from the reference PICC specified in the basic specifications is specified in consideration of the antenna shape and presumed load conditions of PICC, and this reference PICC is used for PCD performance testing.

### (a) Dimensions of the Reference PICCs

The Reference PICCs shall consist of an area containing the coils which has the height and width defined in ISO/IEC 7810 for ID-1 type. An area external to this, containing the circuitry which emulates the required PICC functions, shall be appended in such a way as to allow insertion into the test set-ups described below and so as to cause no interference to the tests. The dimensions shall be as in "Fig. 15.2-4 Reference PICC Dimensions".

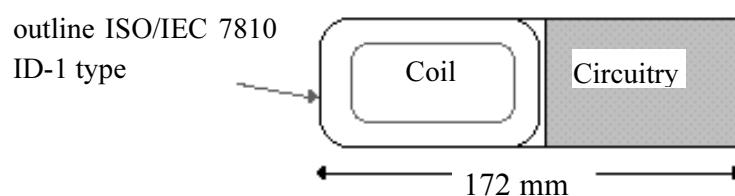


Fig. 15.2-4 Reference PICC Dimensions

### (b) Thickness of Reference PICC Board

The thickness of the reference PICC active area shall be  $0.76 \text{ mm} \pm 10\%$ .



## (c) Coil Characteristics

The characteristics of the reference PICC coil are shown in "Table 15-2-5 Reference PICC Coil Characteristics".

Table 15-2-5 Reference PICC Coil Characteristics

Item	Description		
	Reference PICC - S	Reference PICC - L	Reference PICC (basic specifications)
Coil dimensions	66.6 mm $\pm$ 2% x 31 mm $\pm$ 2%, corner R 8.5 mm $\pm$ 2% (coil inner diameter dimensions)	83.6 mm $\pm$ 2% x 52 mm $\pm$ 2%, corner R 5 mm $\pm$ 2% (coil outer diameter dimensions)	72 mm $\pm$ 2% x 42 mm $\pm$ 2%, corner R 5 mm $\pm$ 2% (coil outer diameter dimensions)
Pattern width	0.5 mm $\pm$ 20%	Same as left	Same as left
Pattern interval	0.5 mm $\pm$ 20%	Same as left	Same as left
Pattern material	Copper foil	Same as left	Same as left
Pattern thickness	35 $\mu$ m	Same as left	Same as left
No. of turns	4 turns	Same as left	Same as left
Test circuit for evaluation of power transmission	Same as extended specifications	Same as left	-
Test circuit for evaluation of load modulation	Same as extended specifications	Same as left	-

(d) Circuit Drawing

a) Reference PICC for Power Transmission Testing

The circuit drawing of the power transmission testing reference PICC is shown in "Fig. 15.2-5 Schematic of Power Transmission Testing Reference PICC", while the components list is shown in "Table 15.2-6 Components List".

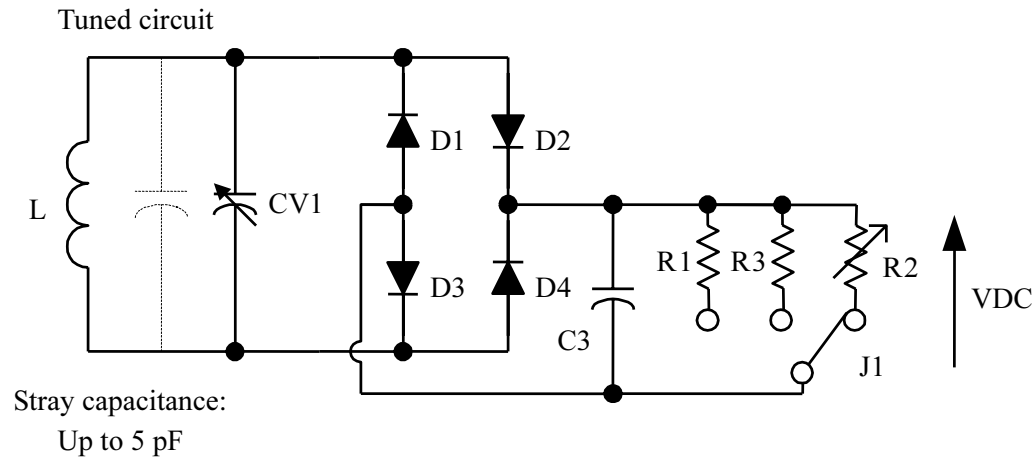


Fig. 15.2-5 Schematic of Power Transmission Testing Reference PICC

Table 15.2-6 Components List

Component	Specifications
L (Coil)	See (e) Coil Characteristics
CV1	6-60 pF
C3	10 nf
D1, D2, D3, D4	See Table 15.2-2 (BAR43 or equivalent)
R1	1.8 kOhm (5 mW)
R2	0-5 kOhm
R3	910 Ohm

## b) Reference PICC for load modulation test

The schematic for the reference PICC for load modulation testing is shown in "Fig. 15.2-6 Schematic of Reference PICC for load modulation test", the components for adjusting characteristics are shown in "Table 15-2-7 Pseudo-Circuit Regulatory Part List", and fixed components are shown in "Table 15-2-8 Components List".

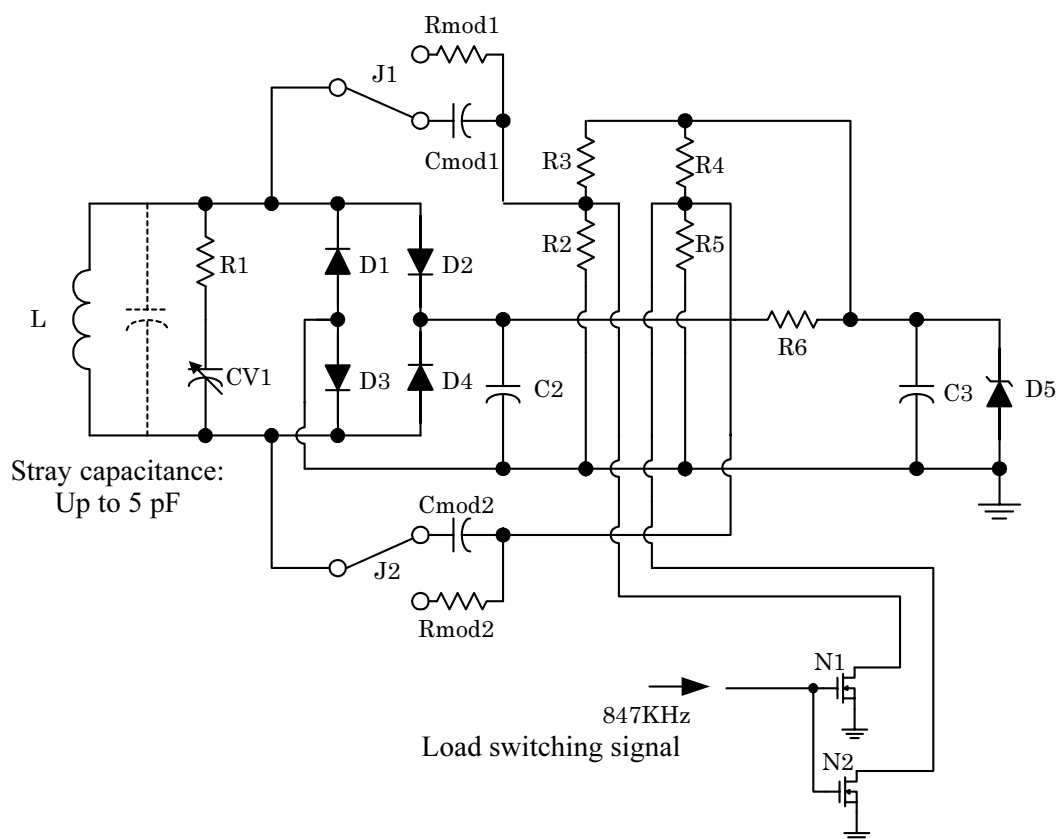


Fig. 15.2-6 Schematic of Reference PICC for load modulation test

Table 15-2-7 Pseudo-Circuit Regulatory Part List

Component	Function	Specifications
R1	adjust Q	0 Ohm
CV1	adjust Resonance	Resonance frequency: 19 MHz
Cmod1, Cmod1	Capacitive modulation	None
Rmod1, Rmod2	Resistive modulation	A resistance value shall be selected that serves as the load modulation amplitude specified in "10.1.2 Load Modulation" or "10.2.2 Load Modulation".
R6	Shunt Current	100 Ohm
D5	Shunt Voltage	5.1 V

Table 15-2-8 Components List

Component	Specifications
R2	1 MOhm
R3	1 MOhm
R4	1 MOhm
R5	1 MOhm
D1, D2, D3. D4	See Table 15.2-2 (BAR43 or equivalent)
L (Coil)	See (e) Coil Characteristics
CV1	6-60 pF
C2	100 pF
C3	10 nF
N1, N2	N-MOS transistor (ground capacitance of 10 pF or less)

c) Reference PICC for Modulation Waveform Testing

The schematic of the reference PICC for modulation waveform testing is shown in "Fig. 15.2-7 Schematic of Reference PICC for Modulation Waveform Testing", while the components list is shown in "Table 15-2-9 Components List".

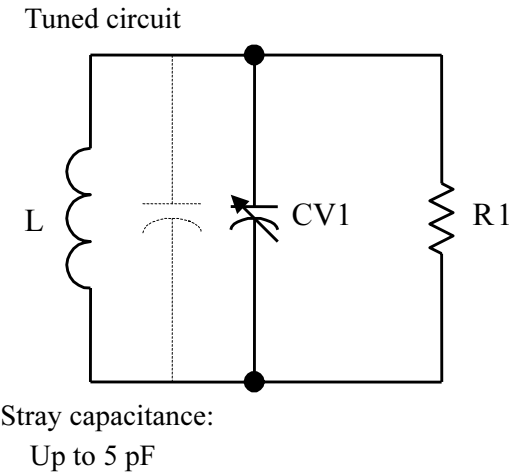


Fig. 15.2-7 Schematic of Reference PICC for Modulation Waveform Testing

Table 15-2-9 Components List

Part	Specifications
L (Coil)	See (e) Coil Characteristics
CV1	6-60 pF
R1	910 Ohm

(3) References

None

## 15.3 Test Methods

### 15.3.1 Magnetic Field Strength

This test measures the magnetic field strength generated by the PCD.

#### (1) Basic Specifications

The strength of the magnetic field generated by the PCD within the operating range of the PCD is measured. In this test, a magnetic field is set with the reference PICC under the conditions of (1) through (3) of the following section, and the magnetic field generated by the PCD is confirmed to not exceed the value specified in "8.2.2 PCD Generated Magnetic Field".

(Note: The test is performed with the reference PICC set as the load in the PCD.)

(a) Test Method

a) Maximum Generated Magnetic Field

- 1) Calibrate the magnetic field generated by the test PCD to the value of the maximum generated magnetic field on the calibration coil.
- 2) Adjust the resonance frequency of the reference PICC to 19 MHz.  
(Note: The resonance frequency of the reference PICC is measured with an impedance analyzer or a LCR-meter connected to a calibration coil. The reference PICC coil shall be placed concentric with the calibration coil and positioned as closely as possible. The resonance frequency shall be a frequency at which the reactance component of impedance reaches a maximum.)
- 3) The reference PICC shall be placed in the DUT position of the test PCD. Set the jumper to connect R2, measure the voltage at both ends of R2 with a high impedance voltmeter, and adjust the voltage to 3 Vdc. Observe the change in the state of the operating magnetic field by monitoring the voltage generated on the calibration coil.
- 4) Place the reference PICC within the operating range of the measured PCD. The voltage at both ends of R2 shall not exceed 3 Vdc when measured with a high impedance voltmeter.

b) Minimum Generated Magnetic Field

- 1) Calibrate the magnetic field generated by the test PCD to the value of the minimum generated magnetic field on the calibration coil.
- 2) Adjust the resonance frequency of the reference PICC to 13.56 MHz.
- 3) The reference PICC shall be placed in the DUT position of the test PCD. Set the jumper to connect R2, measure the voltage at both ends of R2 with a high impedance voltmeter, and adjust the voltage to 3 Vdc. Observe the change in the state of the operating magnetic field by monitoring the voltage generated on the calibration coil.
- 4) Place the reference PICC within the operating range of the measured PCD. The voltage at both ends of R2 shall exceed 3 Vdc when measured with a high impedance voltmeter.

(b) Measurements

The voltage  $V_{dc}$  in the minimum generated magnetic field and maximum generated magnetic field is measured.

(c) Specifications

a) Maximum generated magnetic field

Receive voltage of 3 V or less within the operating range of the PCD.

b) Minimum generated magnetic field

Receive voltage of 3 V or more within the operating range of the PCD.

(2) Extended Specifications

(a) Measurement Using Reference PICC

a) Test Method

Measure the minimum generated magnetic field and maximum generated magnetic field using the reference PICC-S and reference PICC-L specified in the extended specifications of "15.2.1. Reference PICC".

The test method is the same as that of the basic specifications.

b) Measurements

Measurements are the same as those of the basic specifications.

c) Specifications

1) Maximum generated magnetic field

Receive voltage of 3 V or less within the operating range of the PCD.

2) Minimum generated magnetic field

Receive voltage of 3 V or more within the operating range of the PCD.



(b) Measurement Using Calibration Coil

a) Test Method

Measure the magnetic field within the operating range of the PCD with the calibration coil (basic specifications) specified in "14.2.1 Calibration Coil".

b) Measurements

The maximum magnetic field and minimum magnetic field within the operating range of the PCD are measured.

c) Specifications

1) Maximum generated magnetic field

Must be equal to or less than the maximum operating magnetic field specified in "8.2.2 PCD Generated Magnetic Field".

2) Minimum generated magnetic field

Must be equal to or greater than the minimum operating magnetic field specified in "8.2.2 PCD Generated Magnetic Field".

(3) References

None

### 15.3.2 Power Transmission Test

This test is conducted to confirm that the PCD is able to supply the required power to the PICC no matter where the PICC is placed in the operating range of the PCD.

#### (1) Basic Specifications

##### (a) Test Method

Connect a jumper to resistor R1 of the reference PICC and adjust the resonance frequency of the reference PICC to 19 MHz. Measure the voltage generated at both ends of R1 with a high impedance voltmeter.

##### (b) Measurements

The voltage generated at both ends of R1 is measured within the operating range of the PCD.

##### (c) Specifications

Receive voltage of reference PICC: 3 V or more

#### (2) Extended Specifications

None

#### (3) References

##### (a) Test Method

Measure using the reference PICC for power transmission testing specified in the extended specifications of "15.2.1 Reference PICC".

The test method is the same as that of the basic specifications.

##### a) Measurement with a single reference PICC

Connect a jumper to resistor R3 of the reference PICC and adjust the resonance frequency to 19 MHz. Measure the voltage generated at both ends of R3 with a high impedance voltmeter. Measurement is performed with all reference PICCs.

##### b) Measurement with 2 superimposed reference PICC

This test only applies to the slot-in type PCD.

Connect a jumper to resistor R3 of the reference PICC and adjust the resonance frequency to 19 MHz. (Adjust for the two reference PICCs used in testing.)

Place the reference PICCs in the operating range of the PCD while superimposed on each other and measure the voltage generated at both ends of R3 with a high impedance voltmeter.

Check for all combinations of reference PICCs.

(b) Measurements

The voltage generated at both ends of R3 is measured within the operating range of the PCD.

(c) Specifications

Receive voltage of reference PICC: 6.8 V or more

### 15.3.3 Modulation Waveform

This test measures the modulation factors, the rise and fall times, and overshoot values based on the waveform sent out by the PCD.

#### (1) Basic Specifications

##### (a) Test Method

Place the calibration coil in the operating magnetic field region of the PCD, observe the voltage waveform induced on the coil displayed on an oscilloscope screen, and measure the modulation factor and waveform characteristics.

##### (b) Measurements

The modulation waveform in the operating range of the PCD is measured, along with measurement of the modulation factor, rise time, fall time, and overshoot.

##### (c) Specifications

The modulation factor and modulation waveform shall satisfy the specifications of "9.1.2 Modulation".

#### (2) Extended Specifications

The modulation waveform is measured with the reference PICC is set in place.

##### (a) Test Method

Measure the modulation waveform on the calibration coil with the reference PICC placed within the operating range of the PCD.

Perform measurement using the reference PICC for modulation waveform testing specified in the extended specifications of "15.2.1 Reference PICC".

##### a) Measurement with a single reference PICC

The test method is as described below.

- 1) Adjust the reference PICC so as to synchronize at 19 MHz.
- 2) Place the calibration coil over the reference PICC coil, place the reference PICC in the operating range of the PCD, and measure the modulation waveform by monitoring the voltage waveform induced on the calibration coil.

b) Testing with 2 superimposed reference PICC

This test applies only to the slot-in type PCD. The test method is as described below.

- 1) Adjust the reference PICC so as to synchronize at 19 MHz. (Adjust for both reference PICCs used in testing.)
- 2) Place the calibration coil over the reference PICC coil with the two reference PICCs superimposed over each other, place the reference PICCs in the operating range of the PCD, and measure the modulation waveform by monitoring the voltage waveform induced on the calibration coil.

(b) Measurements

The modulation waveform in the operating range of the PCD is measured along with measurement of the modulation factor, rise time, fall time, and overshoot.

(c) Specifications

The degree of modulation and modulation waveform shall satisfy the specifications of "9.1.2 Modulation".

(3) References

None

### 15.3.4 Reception Ability of Load Modulation Signal

#### (1) Basic Specifications

##### (a) Test Method

This test verifies that the load modulation signal of the PICC is able to be properly demodulated by the PCD. The PCD is judged as being normal when it properly receives the subcarrier signal generated from the load modulation testing reference PICC .

Measure the load modulation signal reception ability of the PCD with the load modulation testing reference PICC specified in "15.2.1 Reference PICC".

This reference PICC is calibrated within the magnetic field strength generated by the test PCD so that conditions are not set ignoring various PCDs. This value shall be equal to the magnetic field strength generated by the actual PCD. The magnetic field generated by the PCD is measured using the calibration coil.

##### (b) Measurements

The load modulation signal that can be received by the PCD within the operating range of the PCD is measured.

##### (c) Specifications

The load modulation signal specified in "10.1.2 Load Modulation" must be able to be received within the operating range of the PCD.

(2) Extended Specifications

(a) Test Method

Measure with the load modulation testing reference PICC specified in the extended specifications of "15.2.1 Reference PICC".

Other parts of the test method are the same as the basic specifications.

(b) Measurements

The load modulation signal that can be received by the PCD within the operating range of the PCD is measured.

(c) Specifications

The load modulation signal specified in "10.1.2 Load Modulation" must be able to be received within the operating range of the PCD.

(3) References

None

## 16. External Communication Protocol

This clause specifies commands and responses that are required for realizing a proximity communication interface in the communication protocol between the PCD and an external device (to be referred to as an "upper device"). An external communication protocol that is capable of realizing both type A and type B communication formats on a single PCD is specified.

The anticollision processing method for type A PICC shall be the time slot method. The anticollision processing method for type B cards shall also be the time slot method.

With respect to the external communication protocol, the contents described in "16. External Communication Protocol" provided as reference specifications since this is not specified in ISO/IEC 14443.

### 16.1 Physical Interface

The specifications of the physical interface between the PCD and upper device are shown in "Table 16.1-1 Physical Interface Specifications".

Items in the table other than communication speed are fixed and cannot be changed. Details of the method for changing the communication speed are described in "16.5.3 (4) Changing Upper Communication Speed".

Table 16.1-1 Physical Interface Specifications

Item		Specifications
Signal level		RS-232C
Synchronization method		Half-duplex asynchronous
Flow control		None
Connector type (on PCD)		D-SUB9 pin (male)
Pin configuration (on PCD)		See "Table 16.1-2 Pin Configuration"
Character format (see "Fig. 16.1-1 Character Transmission Format")	Start bit	1 bit
	Data bits	8 bits (LSB first)
	Parity bit	Even parity
	Stop bit	1 bit
Communication speed		9600bps ~ 115200bps (initial value: 9600 bps)



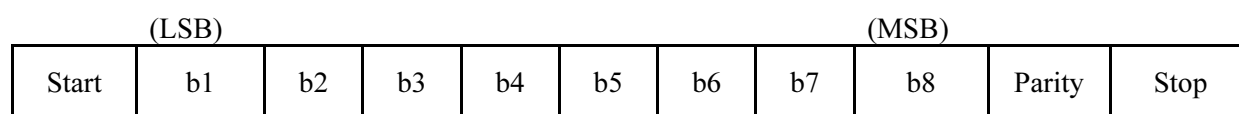
The pin configuration of the connector of the PCD to which the external device is connected is shown in "Table 16.1-2 Pin Configuration".

Table 16.1-2 Pin Configuration

Pin no.	Signal	Input/output*	Meaning
1	CD	Input	(Not used)
2	RD	Input	Data received from upper device
3	SD	Output	Data sent to upper device
4	ER	Output	On (fixed)
5	SG	-	Signal ground
6	DR	Input	(Not used)
7	RS	Output	On (fixed)
8	CS	Input	(Not used)
9	RI	Input	(Not used)

\* The direction of input and output in the table is the direction as viewed from the PCD.

The character transmission format is shown in "Fig. 16.1-1 Character Transmission Format".



(transmitted first)

Fig. 16.1-1 Character Transmission Format

# 16.2Block Format

Communication between an upper device and PCD is performed in block units. Blocks are always sent by the upper device to the PCD first. Blocks sent from the upper device to the PCD are referred to as command blocks or commands.

When the PCD receives a command block from an upper device, it processes the command block and, as a general rule, returns the results to the upper device. Blocks sent from the PCD to the upper device are referred to as response blocks or simply as responses.

The format of command blocks and response blocks is shown in "Fig. 16.2-1 Block Format". Items surrounded by brackets "[ ]" in the figure indicate optioned items, and may not be transmitted depending on block contents. Items surrounded by parentheses "( )" in the figure represent the number of bytes for that item. Blocks are transmitted from left to right in the figure during block transmission.

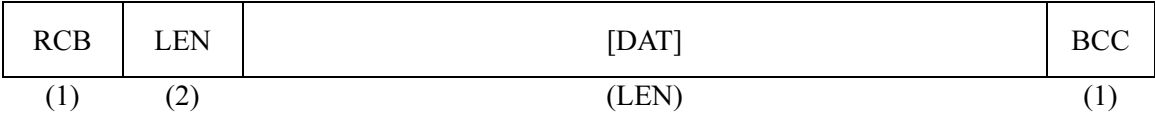


Fig. 16.2-1 Block Format

### 16.2.1 RCB (Required)

RCB is a single byte of data that indicates the type of block transmitted. It indicates the type of command in command blocks sent from the upper device to the PCD, or, in a response block returned to the upper device from the PCD, indicates the receive state of the command block received immediately before.

RCB encoding and its contents are shown in "Table 16.2-1 Upper Device to PCD" and "Table 16.2-2 PCD to Upper Device".

Table 16.2-1 Upper Device to PCD

b8	b7	b6	b5	b4	b3	b2	b1	Description
0	0	-	-	-	-	-	-	Command for PICC (DAT portion sent to PICC)
0	1	-	-	-	-	-	-	Command for PCD (DAT portion processed with PCD)
1	-	-	-	-	-	-	-	Request to resend response (request to resend immediately prior response. The contents of the DAT portion are ignored)

Dashes "-" are retained for future specification and have a value of '0'.

Table 16.2-2 PCD to Upper Device

b8	b7	b6	b5	b4	b3	b2	b1	Description
0	-	-	-	-	-	-	-	Normal command reception
1	-	-	-	-	-	0	0	Character receive error (parity error, framing error, overrun, etc.)
1	-	-	-	-	-	0	1	CWT error (insufficient data received)
1	-	-	-	-	-	1	0	Receive buffer overflow
1	-	-	-	-	-	1	1	BCC error

Dashes "-" are retained for future specification and have a value of '0'.

### 16.2.2 LEN (Required)

LEN consists of two bytes of data that indicate the size of the DAT portion in a transmitted block. LEN has a value of 0000h to 0103h, and the upper byte is transmitted first.

When the PCD receives a command block from an upper device, the first three bytes are received as RCB and LEN. Next, data of the number of bytes indicated with LEN is read as DAT, and the next byte is processed as BCC.

If BCC is judged as normal, the contents of the received command block are interpreted and processing is carried out.

If the value of LEN in a command block is greater than the actual size of the DAT portion, the PCD judges that the data has been interrupted during the course of receiving. When this happens, the PCD shall return a response block indicating a CWT error to the upper device.

In addition, in the case the value of LEN is 0104h or more and the length of the DAT portion actually received is 0104h or more, the amount of received data may overflow from the receive buffer of the PCD. When this happens, PCD shall return a response block indicating a receive buffer overflow error to the upper device.

### 16.2.3 DAT (Optional)

DAT is data of variable length that indicates the main body of a command or response. Details of DAT encoding are defined in "16.5 Commands and Responses".

DAT is optional and there are blocks that do not contain DAT. Blocks without DATs are, resend response request blocks character receive error blocks, CWT error blocks, receive buffer overflow blocks and BCC error blocks. B8 of RCB is set to '1' in these blocks. (For details, refer to "16.2.1 RCB (Required)").

#### 16.2.4 BCC (Required)

BCC is a single byte of data that indicates the block check code. The value of BCC is encoded so that the bitwise exclusive OR with RCB will result in a value of 00h.

If the result of calculating BCC is other than 00h, the PCD judges that receiving of the command block has failed. When this happens, the PCD sends a response block indicating a BCC error to the upper device.

### 16.3 Communication Time Specifications

Specification of the maximum delay time between characters within a block (character waiting time, CWT) is shown in "Fig. 16.3-1 Timing Between Characters" with respect to specification of the communication time between an upper device and PCD.

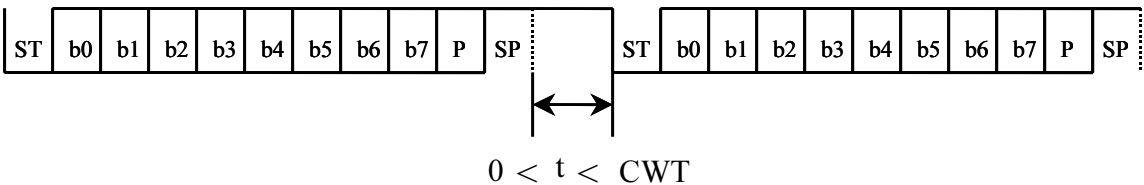


Fig. 16.3-1 Timing Between Characters

In addition, specification of block guard time (BGT) and specification of block waiting time (BWT) are shown in "Fig. 16.3-2 Timing Between Blocks".

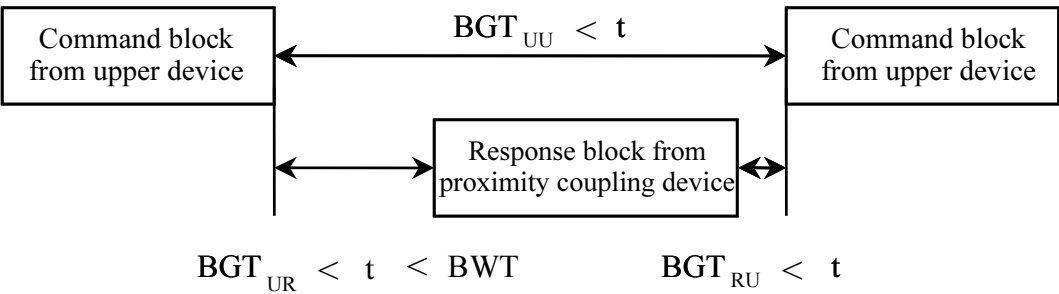


Fig. 16.3-2 Timing Between Blocks

### 16.3.1 Character Waiting Time (CWT)

The maximum delay time between two consecutive characters within a single block is shown in "Table 16.3-1 Character Waiting Time (CWT)". If the amount of time between two consecutive characters while receiving a block exceeds CWT, an inter-character timeout occurs.

If the PCD detects an inter-character timeout while receiving a command block from an upper device, it returns a CWT error block to the upper device.

Recommended processing when the upper device detects an inter-character timeout while receiving a response block from the PCD consists of interrupting the receive processing and sending a resend request block .

Table 16.3-1 Character Waiting Time (CWT)

Symbol	Maximum time (ms)
CWT	50

The minimum delay time between characters is 0 ms.



### 16.3.2 Block Guard Time (BGT)

Block guard time (BGT) is the shortest amount of time between two consecutive blocks along the transmission path between an upper device and PCD. If the next block is transmitted before BGT has elapsed, that block is not guaranteed.

The following three types of BGT are defined.

- $BGT_{UR}$ : Shortest amount of time until the PCD sends a response block in response to a command block from an upper device
- $BGT_{RU}$ : Shortest amount of time until an upper device sends a command block in response to a response block from the PCD
- $BGT_{UU}$ : Shortest amount of time to send command blocks consecutively from an upper device. These specifications are not applied in cases where a response block from the PCD is present between consecutive command blocks. (See "16.4.1 (6) Consecutive Command Receive Error")

The value of each BGT is shown in "Table 16.3-2 Block Guard Time (BGT)".

Table 16.3-2 Block Guard Time (BGT)

Symbol	Minimum time (ms)
$BGT_{UR}$	1
$BGT_{RU}$	1
$BGT_{UU}$	CWT + 10 or BWT <sub>UR</sub> , whichever is longer

### 16.3.3 Block Waiting Time (BWT)

The maximum waiting time until a response block from the PCD is started to be received following completion of transmission of a command block from an upper device is shown in "Table 16.3-3 Block Waiting Time (BWT)". If the amount of time until the start of block receiving exceeds BWT, an inter-block timeout occurs. Refer to "16.4.2(3) Receive Timeout (BWT)" for information on processing when the upper device detects an inter-block timeout.

BWT can have three types of values depending on the type of RCB of the command block sent from the upper device.

Table 16.3-3 Block Waiting Time (BWT)

Symbol	Conditions	Maximum time (ms)
BWT	Command for PICC	Transmission time to PICC + maximum receive waiting time of PICC + receive time from PICC + 10
	Command for PCD	500
	Resend response request	10

The maximum waiting time until the start of receiving of a command block from an upper device following completion of sending a response block by the PCD is not specified.  
(The PCD does not monitor the waiting time of command blocks.)

## 16.4 Communication Error Processing

Processing by the PCD and processing by the upper device when an error occurs during communication between the upper device and PCD are as described below.

### 16.4.1 PCD Communication Error Processing

The processing of the PCD when a receive error occurs in the PCD is as described below.

#### (1) Character Receive Error

If there is an error in a character received by the PCD (such as a parity error, framing error or overrun), a character receive error occurs.

If the PCD has successfully received data through LEN, a character receive error block is returned to the upper device following reception through BCC. If a character receive error occurs during reception of RCB or LEN, the PCD treats this as receiving noise, discards the portion it has received up to that point, and repeats reception from the beginning.

#### (2) CWT Error

If an inter-character timeout occurs while there is data still remaining to be received, a CWT error occurs. If the PCD has successfully received data through LEN, an CWT error block is immediately returned to the upper device. If the an error occurred prior to receiving LEN, the PCD treats this as receiving noise and repeats reception from the beginning.

#### (3) Receive Buffer Overflow

If the data received exceeds the capacity of the receive buffer of the PCD, a receive buffer overflow occurs. When a receive buffer overflow occurs, the PCD discards all received data and immediately returns a receive buffer overflow block to the upper device.

#### (4) BCC Error

The PCD performs a BCC check after receiving data through BCC. If the calculated value of BCC is in error (other than 00h), a BCC error occurs. When a BCC error occurs, the PCD discards all received data and immediately returns a BCC error block to the upper device.

#### (5) Received Data Amount Error

If additional data is received after receiving data through BCC, a received data amount error occurs. When a received data amount error occurs, the PCD performs processing ignoring all the data received after the error. Namely, processing for the received command block is performed if the contents of that command block are normal.

However, the operation of the PCD is not guaranteed when consecutive data is received by the PCD beyond  $BGT_{UR}$ .

#### (6) Consecutive Command Receive Error

Since communication between an upper device and the PCD is half-duplex, the upper device, as a general rule, sends the next command block after having received a response block from the PCD. However, there are cases in which the PCD does not return a response to the upper device for reasons such as a receive error in the PCD or while waiting for a response from a PICC.

In such cases, if a command block is sent from the upper device on or after  $BGT_{UU}$ , the PCD discontinues processing up to that point and performs processing for receiving a new command block. The PCD only sends a response block in response to a new command block and will not send a response block for the processing that was discontinued.

If the PCD receives data prior to  $BGT_{UU}$ , a consecutive command receive error occurs. The operation of the PCD is not guaranteed when a consecutive command receive error occurs.

## 16.4.2 Upper Device Communication Error Processing

The recommended processing by an upper device when a communication error has been detected in the upper device is as described below.

### (1) Receive Error

If some type of error is detected in a response block received from a PCD (such as a character receive error, CWT error or BCC error), a receive error occurs.

If a receive error has been detected in the upper device, a resend response request block is sent to the PCD. When the PCD receives this block, it resends the latest response block that was sent.

If a receive error is detected again in the response to resend response request block, the manager of the upper device shall verify the communication line since there is the possibility of an error in the communication line between the upper device and PCD.

### (2) Error Response Received

If a response received from the PCD is a block that indicates a command block receive error in the PCD (character receive error block, CWT error block or BCC error block), an error response receipt occurs.

When an error response receipt is detected in the upper device, the same as the command block previously sent is resent to the PCD is resended.

If a response error is detected again in response to the resent command, the manager of the upper device shall verify the communication line since there is the possibility of an error in the communication line between the upper device and PCD.

### (3) Receive Timeout (BWT)

If there is no response from the PCD after BWT has elapsed, a receive timeout (BWT) error occurs.

When a receive timeout (BWT) is detected in the upper device, the following processing is performed according to the type of RCB of the command block that was sent.

- If a command for a PICC was sent:  
A PICC communication error is assumed to have occurred, and a command is resent according to the protocol of the PICC.  
Refer to "13. Transmission Protocol" for details regarding the procedure for resending commands to a PICC.
- If a command for the PCD was sent:  
There is the possibility that communication itself may not have been possible. If a receive timeout occurs again after resending the command, check whether or not the power supply to the PCD is normal, and whether an anomaly has occurred in the communication line.  
(In the case of a PCD self-diagnostic command, since specifications are such that a response block is not returned from the PCD, detection of a receive time out (BWT) must not be performed by the upper device.)
- If a resend request response was sent:  
There is the possibility that communication itself may not have been possible. If a receive timeout occurs again after resending the command, check whether or not the power supply to the PCD is normal, and whether an anomaly has occurred in the communication line.

## 16.5 Commands and Responses

Commands are divided into commands for a PICC, commands for the PCD, and resend response request according to the value of RCB. The following provides a description of commands for PICC and commands for PCD along with their responses.

### 16.5.1 Commands and Response for PICC

If the value of b8 and b7 of RCB of a command block sent from an upper device is 0, the command is for a PICC.

When the case the PCD has normally received a command for a PICC, processing is performed according to the procedure described below.

- 1) The DAT portion of the received command block is set in a buffer for sending to the PICC.
- 2) The data in the buffer is sent to the PICC according to the communication frame format with the PICC.
- 3) A response from the PICC is awaited .
- 4) When a response is received from the PICC, only the data is extracted from the communication frame and set in the receive buffer.
- 5) The contents of the receive buffer are set in the DAT portion of the response block.
- 6) RCB, LEN and BCC are calculated, and a response block is sent to the upper device.

When communicating with a PICC using a command for a PICC, the precautions described below must be taken in the upper device.

- Prior to starting communication with the PICC, the carrier output from the PCD shall be turned on with a command for the PCD (carrier control command: see "16.5.3 (5) Carrier Control" for details).
- Communication conditions between the PCD and PICC are set with a command for the PCD (PICC communication information setting command: see "16.5.3 (6) PICC Communication Information Setting " for details).
- If CRC is used in communication with a PICC, since CRC is not calculated in the PCD, the CRC that will be sent to the PICC shall be embedded in advance in the DAT portion of the command for a PICC. In addition, the CRC received from the PICC shall also be contained in the response block.
- The PCD waits for a response from the PICC until a response is detected from the PICC. Consequently, if there is no response from the PICC, the PCD does not return a response block to the upper device.
- If the PCD detects an error when receiving a command from an upper device, it returns a receive error response block to the upper device without sending the DAT portion to the PICC.



The initial values of communication settings between the PCD and PICC are shown in "Table 16.5-1 PICC Communication Setting Initial Values".

Table 16.5-1 PICC Communication Setting Initial Values

Item	Initial value
PICC type	Type B
Communication speed (PCD to PICC)	106 kbps
Communication speed (PICC to PCD)	106 kbps

Processing when the PCD detects a communication error while receiving a response from the PICC is shown in "Table 16.5-2 Error Processing when Receiving Response from PICC".

Table 16.5-2 Error Processing when Receiving Response from PICC

Status	Processing
Character receive error prior to normal character reception	Treated as reception of noise and reception is continued.
Character receive error after normal character reception	Reception terminated and portion received normally sent to upper device.
Receive buffer overflow (FSD)	Reception termination through FSD and received portion sent to upper device.
(CRC error)	CRC error does not occur since CRC check not performed.
(FWT error)	FWT error does not occur since FWT monitoring not performed

## 16.5.2 Summary of Commands and Responses for PCD

### (1) Summary of Commands for PCD

If b8 of RCB is 0 and b7 is 1, processing is performed as command for the PCD.

The format of the DAT portion of command blocks in commands for the PCD is shown in "Fig. 16.5-1 Command DAT Portion Format". Each item of the DAT portion is sent from left to right when sending commands.

Items surrounded by brackets "[ ]" in the figure refer optional items, and may not be added depending on the command. Items surrounded by parentheses "( )" represent the number of bytes of that item.

CLA	INS	P1	P2	[Lc]	[Data]	[Le]
(1)	(1)	(1)	(1)	(1)	(Lc)	(1)

Fig. 16.5-1 Command DAT Portion Format

In addition, the meaning of each item in the DAT portion block within a command block in commands for the PCD is shown in "Table 16.5-3 Meanings of Items".

Table 16.5-3 Meanings of Items

Item	Meaning
CLA	Command layer. Value is fixed at 00h (other values are retained for future specification).
INS	Command type. Details are shown in "Table 16.5-4 List of INS".
P1	Parameter 1 corresponding to INS.
P2	Parameter 2 corresponding to INS.
Lc	Length of data portion (optional*)
Data	Main body of data sent by PCD (optional*)
Le	Expected length of response data if data length of a response is designable (optional*)

\* Items indicated as being optional may not be added depending on the command.

The correlation between INS values and commands is shown in "Table 16.5-4 List of INS".

Table 16.5-4 List of INS

Value	Command name	Section
01h	PCD Reset	16.5.3 (1) PCD Reset
03h	PCD Information Acquisition	16.5.3 (2) PCD Information Acquisition
05h	PICC Communication Information Acquisition	16.5.3 (3) PICC Communication Information Acquisition
07h	Changing Upper Communication Speed	16.5.3 (4) Changing Upper Communication Speed
11h	Carrier Control	16.5.3 (5) Carrier Control
13h	PICC Communication Information Setting	16.5.3 (6) PICC Communication Information Setting
21h	Request All A	16.5.3 (7) Request All A
23h	Select A	16.5.3 (8) Select A
25h	Request for ATS	16.5.3 (9) Request for ATS
27h	Parameter Change	16.5.3 (10) Parameter Change
29h	Halt A	16.5.3 (11) Halt A
31h	Request All B	16.5.3 (12) Request All B
33h	Attribute	16.5.3 (13) Attribute
39h	Halt B	16.5.3 (14) Halt B
3Bh	Wake-up All B	16.5.3 (15) Wake-up All B
F1h	PCD Self-Diagnosis	16.5.3 (16) PCD Self-Diagnosis
Other	(Retained for future specification)	

## (2) Summary of Responses for PCD

The format of the DAT portion of response blocks in response to commands for the PCD is shown in "Fig. 16.5-2 Response DAT Portion Format". Each item of the DAT portion is sent from left to right when sending a response.

Items surrounded by brackets "[ ]" in the figure refer to optional items, and may not be added depending on the response. Items surrounded by parentheses "( )" represent the number of bytes of that item.

[Data]	SW1	SW2
(fixed value or Le)	(1)	(1)

Fig. 16.5-2 Response DAT Portion Format

In addition, the meaning of each item in the DAT portion block of a response block in response to commands for the PCD is shown in "Table 16.5-5 Meanings of Items".

Table 16.5-5 Meanings of Items

Item	Meaning
Data	Data obtained as a result of executing a command. The length of the data portion is either the value specified by a command or the value indicated with Le in a command (optional*).
SW1	Status word 1. Details of encoding of SW1 are shown in "Table 16.5-6 List of SW".
SW2	Status word 2. Details of encoding of SW2 are shown in "Table 16.5-6 List of SW".

\* Items indicated as being optional may not be added depending on the response.

The possible values of SW1 and SW2 along with their meanings are shown in "Table 16.5-6 List of SW".

Table 16.5-6 List of SW

SW1	SW2	Meaning
90	00	Normal termination
62	00	Warning
62	F0	PICC communication receive timeout
62	F1	PICC communication receive error
64	00	Execution error
67	00	Command length error
69	00	Command not allowed
6B	00	P1, P2 error
6D	00	INS not supported
6E	00	CLA not supported
6F	00	Self-diagnosis error

Although the list of SW indicates all combinations of SW1 and SW2 that can be used in a response by the PCD, depending on the command, there are some SW that are not generated according to a command. (For details, refer to "16.5.3 Details of Commands and Responses for PCD".)

### 16.5.3 Details of Commands and Responses for PCD

#### (1) PCD Reset

##### (a) Operation

The state of the PCD is initialized.

Initialized items are as shown in "Table 16.5-7 Initialized Items". (The upper communication speed is not initialized.)

Table 16.5-7 Initialized Items

Item	Initial value
Carrier control	carrier output off
PICC type	Type B
Communication speed (PCD to PICC)	106 kbps
Communication speed (PICC to PCD)	106 kbps

##### (b) Command Format

The command format of PCD reset is shown in "Fig. 16.5-3 Command Format". Values represented in the form of xxh of each item in the figure indicate encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA	INS	P1	P2
00h	01h	00h	00h
(1)	(1)	(1)	(1)

Fig. 16.5-3 Command Format

Other values of P1 and P2 are retained for future specification.

## (c) Response Format

The response format of PCD reset is shown in "Fig. 16.5-4 Response Format". The values in parentheses "( )" in the figure indicate the number of bytes.

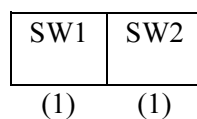


Fig. 16.5-4 Response Format

## (d) Status

The values of status (SW1-SW2) in the response of PCD reset are shown in "Table 16.5-8 Status".

Table 16.5-8 Status

SW1	SW2	Meaning
90	00	Normal termination
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (2) PCD Information Acquisition

## (a) Operation

Specific information of the PCD is acquired.

Items that can be acquired are as shown in "Table 16.5-9 PCD Information".

Table 16.5-9 PCD Information

Item	No. of bytes	Description
Specification no.	1	Specification no. with which the PCD complies. This number is to be 01h if it complies with this specification.
No. of send/receive buffers	1	No. of send and receive buffers of the PCD. Refer to "Fig. 16.5-5 Send/Receive Buffer Coefficients" and "Table 16.5-10 Buffer Coefficient and Buffer Number Correlation Chart" for encoding details.
PICC communication speed	1	Ability of the PCD to accommodate communication speed for the PICC. Refer to "Table 16.5-11 Communication Speeds Supported by PCD" for encoding details.
Type B options	1	Ability to execute options relating to type B communication frames. Refer to "Fig. 16.5-6 Encoding of Type B Options", "Table 16.5-12 Accommodation of Omission of SOF/EOF", "Table 16.5-13 Minimum Value of Subcarrier Non-Modulation Period" and "Table 16.5-14 Minimum Value of Subcarrier Preamble" for encoding details.
Upper communication speed no.	1	Number of bytes of upper communication speed (value of 1 or 2)
Upper communication speed	1 ~ 2	Supported upper communication speed. Maximum communication speed = Basic communication speed $\times 2_n$ Upper 4 bits: Basic communication speed (0: 9600 bps, 1: 14400 bps, other: retained for future specification) Lower 4 bits: Maximum communication speed multiplier n Example) 02h: Supports 9600/19200/38400 bps, 13h: supports 14400/28800/57600/115200 bps
Manufacturer's characteristic data no.	1	Number of bytes of manufacturer specific data.
Manufacturer specific data	0 ~ 8	Number of bytes of PCD manufacturer specific data. Maximum of 8 bytes. Can be used arbitrarily by PCD manufacturers.



The number of send/receive buffers is indicated using buffer coefficients. The encoding format of send/receive buffer coefficients is shown in "Fig. 16.5-5 Send/Receive Buffer Coefficients".

b8	b7	b6	b5	b4	b3	b2	b1
Send buffer coefficient				Receive buffer coefficient			

Fig. 16.5-5 Send/Receive Buffer Coefficients

The correlation between buffer coefficients and the number of buffers is shown in "Table 16.5-10 Buffer Coefficient and Buffer Number Correlation Chart".

Table 16.5-10 Buffer Coefficient and Buffer Number Correlation Chart

Buffer coefficient	'0'	'1'	'2'	'3'	'4'	'5'	'6'	'7'	'8'	'9' - 'F'
Buffer (bytes)	16	24	32	40	48	64	96	128	256	Retained for future specification

The PICC communication speed indicates the ability of the PCD to accommodate the PICC communication speed by using the format shown in "Table 16.5-11 Communication Speeds Supported by PCD".

Table 16.5-11 Communication Speeds Supported by PCD

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
0	0	0	0	0	0	0	0	PCD only supports 106 kbps in bi-directional transmission
1	-	-	-	0	-	-	-	Bi-directional transmission speed forced to be the same
-	-	-	1	0	-	-	-	Supports 212 kbps transmission speed from PICC to PCD
-	-	1	-	0	-	-	-	Supports 424 kbps transmission speed from PICC to PCD
-	1	-	-	0	-	-	-	Supports 847 kbps transmission speed from PICC to PCD
-	-	-	-	0	-	-	1	Supports 212 kbps transmission speed from PCD to PICC
-	-	-	-	0	-	1	-	Supports 424 kbps transmission speed from PCD to PICC
-	-	-	-	0	1	-	-	Supports 847 kbps transmission speed from PCD to PICC

Encoding of type B options is shown in "Fig. 16.5-6 Encoding of Type B Options".

b8	b7	b6	b5	b4	b3	b2	b1
Minimum value of subcarrier non-modulation period		Minimum value of subcarrier preamble		EOF omission accomodation	SOF omission accomodation	Retained for future specification	

Fig. 16.5-6 Encoding of Type B Options

The relationship between values and meanings for accommodation of omission of SOF/EOF is shown in "Table 16.5-12 Accommodation of Omission of SOF/EOF".

Table 16.5-12 Accommodation of Omission of SOF/EOF

b3	SOF omission accomodation	b4	EOF omission accomodation
0	No	0	No
1	Yes	1	Yes

The relationship between the values and meanings for the minimum value of the subcarrier non-modulation period is shown in "Table 16.5-13 Minimum Value of Subcarrier Non-Modulation Period".

Table 16.5-13 Minimum Value of Subcarrier Non-Modulation Period

b8-b7	Minimum value of subcarrier non-modulation period
00	64 / fs
01	48 / fs
10	16 / fs
11	Retained for future specification

The relationship between the values and meanings for the minimum value of the subcarrier preamble is shown in "Table 16.5-14 Minimum Value of Subcarrier Preamble".

Table 16.5-14 Minimum Value of Subcarrier Preamble

b6-b5	Minimum value of subcarrier preamble
00	80 / fs
01	64 / fs
10	16 / fs
11	Retained for future specification

## (b) Command Format

The command format of PCD information acquisition is shown in "Fig. 16.5-7 Command Format". Values represented in the form of xxh for each item in the figure indicate the encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA	INS	P1	P2
00h	03h	00h	00h
(1)	(1)	(1)	(1)

Fig. 16.5-7 Command Format

Other values of P1 and P2 are retained for future specification.

## (c) Response Format

The response format of PCD information acquisition is shown in "Fig. 16.5-8 Response Format". Values in parentheses "( )" in the figure indicate the number of bytes.

Data	SW1	SW2
(7~16)	(1)	(1)

Fig. 16.5-8 Response Format

The contents of the data portion are as shown in "Table 16.5-9 PCD Information". The order of sending is the order in which the items are shown, starting with specification number followed by no. of send/receive buffers and ending with manufacturer specific data. However, in the case the manufacturer's specific data number is 00h, there is no manufacturer specific data.

If the contents of status as indicated with SW1 and SW2 are that other than normal termination, the data portion is not present in the response.

## (d) Status

The values of status (SW1-SW2) in the response of PCD information acquisition are shown in "Table 16.5-15 Status".

Table 16.5-15 Status

SW1	SW2	Meaning
90	00	Normal termination
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (3) PICC Communication Information Acquisition

## (a) Operation

The current PICC communication setting information of the PCD is acquired.

Items that can be acquired are as shown in "Table 16.5-16 PICC Communication Information".

Table 16.5-16 PICC Communication Information

Item	No. of bytes	Description
PICC type	1	00h: Type B, 01h: Type A time slot type. Other values are retained for future specification.
PICC communication speed	1	Encoding details are shown in "Fig. 16.5-9 Encoding of PICC Communication Speed" and "Table 16.5-17 Communication Speed Coefficient and Communication Speed Correlation Chart".

Encoding of PICC communication speed is shown in "Fig. 16.5-9 Encoding of PICC Communication Speed".

b8	b7	b6	b5	b4	b3	b2	b1
(0000)b Other values are retained for future specification.				Communication speed coefficient from PICC to PCD		Communication speed coefficient from PCD to PICC	

Fig. 16.5-9 Encoding of PICC Communication Speed

The correlation between communication speed coefficient and communication speed is shown in "Table 16.5-17 Communication Speed Coefficient and Communication Speed Correlation Chart".

Table 16.5-17 Communication Speed Coefficient and Communication Speed Correlation Chart

Communication speed coefficient	'0'	'1'	'2'	'3'
Communication speed (bytes)	106 kbps	212 kbps	424 kbps	847 kbps

## (b) Command Format

The command format of PCD information acquisition is shown in "Fig. 16.5-10 Command Format". Values indicated in the form of xxh for each item in the figure indicate the encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA	INS	P1	P2
00h	05h	00h	00h
(1)	(1)	(1)	(1)

Fig. 16.5-10 Command Format

Other values of P1 and P2 are retained for future specification.

## (c) Response Format

The response format of PCD information acquisition is shown in "Fig. 16.5-11 Response Format". Values in parentheses "( )" in the figure indicate the number of bytes.

Data	SW1	SW2
(2)	(1)	(1)

Fig. 16.5-11 Response Format

The contents of the data portion are as shown in "Table 16.5-16 PCD Information". The order of sending is the order in which the items are shown, starting with PICC type followed by PICC communication speed.

If the contents of status as indicated with SW1 and SW2 are that other than normal termination, the data portion is not present in the response.

## (d) Status

The values of status (SW1-SW2) in the response of PICC information acquisition are shown in "Table 16.5-18 Status".

Table 16.5-18 Status

SW1	SW2	Meaning
90	00	Normal termination
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

#### (4) Changing Upper Communication Speed

##### (a) Operation

The communication speed between the PCD and an upper device is changed. Communication speeds that can be set are the supported communication speeds obtained with the PCD information acquisition command.

Conditions for changing the PCD to the set communication speed are only when SW1-SW2 are 9000h. In addition, the communication speed of the PCD can only be changed within BGT<sub>RU</sub> after sending a response.

##### (b) Command Format

The command format for changing upper communication speed is shown in "Fig. 16.5-12 Command Format". Values represented in the form of xxh of each item in the figure indicate the encoding of that item, and values in parentheses "( )" indicate the number of bytes.

CLA 00h	INS 07h	P1	P2 00h
(1)	(1)	(1)	(1)

Fig. 16.5-12 Command Format

The value of P1 indicates the communication speed that is set. Encoding of P1 is as shown in "Table 16.5-19 Encoding of Upper Communication Speed", and undefined values are retained for future specification.

The value of P2 is fixed at 00h, and other values are retained for future specification.

Table 16.5-19 Encoding of Upper Communication Speed

Upper 4 bits	Basic communication speed	Lower 4 bits	Communication speed multiplier
0	9600 bps	n	2 <sup>n</sup>
1	14400 bps		

Upper communication speed = Basic communication speed x Communication speed multiplier

## (c) Response Format

The response format for changing upper communication speed is shown in "Fig. 16.5-13 Response Format". Values in parentheses "( )" in the figure indicate the number of bytes.

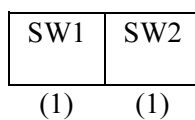


Fig. 16.5-13 Response Format

## (d) Status

The values of status (SW1-SW2) in the response for changing upper communication speed are shown in "Table 16.5-20 Status".

Table 16.5-20 Status

SW1	SW2	Meaning
90	00	Normal termination
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (5) Carrier Control

## (a) Operation

This command controls the on/off state of carrier output from the PCD. States that can be set relating to carrier control are shown in "Table 16.5-21 Carrier States".

Table 16.5-21 Carrier States

Setting	P1
Carrier output off	00h
Carrier output on	01h

## (b) Command Format

The command format of carrier control is shown in "Fig. 16.5-14 Command Format". Values represented in the form of xxh for each item in the figure indicate the encoding of each item, while values in parentheses "( )" indicate the number of bytes.

CLA 00h	INS 11h	P1	P2 00h
(1)	(1)	(1)	(1)

Fig. 16.5-14 Command Format

The values of P1 are as shown in "Table 16.5-21 Carrier States". Furthermore, other values of P1 are retained for future specification.

The value of P2 is fixed at 00h, and other values are retained for future specification.

## (c) Response Format

The response format of carrier control is shown in "Fig. 16.5-15 Response Format". Values in parentheses "( )" in the figure indicate the number of bytes.

SW1	SW2
(1)	(1)

Fig. 16.5-15 Response Format



## (d) Status

The values of status (SW1-SW2) in the response of carrier control are shown in "Table 16.5-22 Status".

Table 16.5-22 Status

SW1	SW2	Meaning
90	00	Normal termination
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (6) PICC Communication Information Setting

## (a) Operation

Communication information of the PCD for the PICC is set. Items that can be set are shown in "Table 16.5-23 PICC Information".

Table 16.5-23 PICC Information

Item	Parameter	Description
PICC type	P1	00h: Type B, 01h: Type A time slot type. Other values are retained for future specification.
PICC communication speed	P2	Encoding details are shown in "Fig. 16.5-9 Encoding of PICC Communication Speed" and "Table 16.5-17 Communication Speed Coefficient and Communication Speed Correlation Chart".

## (b) Command Format

The command format of PICC communication information setting is shown in "Fig. 16.5-16 Command Format". Values represented in the form of xxh for each item in the figure indicate the encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA 00h	INS 13h	P1	P2
(1)	(1)	(1)	(1)

Fig. 16.5-16 Command Format

The values of P1 and P2 are as shown in "Table 16.5-23 PICC Information". However, in the case the PICC type is type A, modulation format from the PCD may show anomaly at PICC communication speeds of 212, 424 and 847 kbps, hence those settings are prohibited. Furthermore, other values of P1 and P2 are retained for future specification.

## (c) Response Format

The response format of PICC communication information setting is shown in "Fig. 16.5-17 Response Format". Values in parentheses "( )" in the figure indicate the number of bytes.

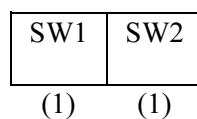


Fig. 16.5-17 Response Format

## (d) Status

The values of status (SW1-SW2) in the response of PICC communication information setting are shown in "Table 16.5-24 Status".

Table 16.5-24 Status

SW1	SW2	Meaning
90	00	Normal termination
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (7) Request All A

## (a) Operation

A single REQA\_t command and REQ-ID command is sent to a type A PICC from a PCD and a returned unique identifier (UID) of a PICC in a normally received ATQ-ID is sent to an upper device. If the UID was not received normally from the PICC, only the collision detection result is returned to the upper device.

(Refer to "12.5 Type A Timeslot - Initialization and Anticollision" for details regarding REQA\_t and REQ-ID.)

When executing this command, parameters are set to the type A time slot type and a communication speed of 106 kbps regardless of the PICC communication settings. Following execution of this command, the PICC communication settings return to their original settings.

## (b) Command Format

The command format of request all A is shown in "Fig. 16.5-18 Command Format". Values represented in the form of xxh of each item in the figure indicate the encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA	INS	P1	P2
00h	21h		
(1)	(1)	(1)	(1)

Fig. 16.5-18 Command Format

The values of P1 and P2 are the same as P1 and P2 of the REQ-ID command sent to the type A PICC.

## (c) Response Format

The response format of request all A is shown in "Fig. 16.5-19 Response Format". The values in parentheses "( )" indicate the number of bytes.

Data	SW1	SW2
()	(1)	(1)

Fig. 16.5-19 Response Format

The format of the data portion in a response block is shown in "Fig. 16.5-25 Data Portion Format". The order of transmission is the same as the order in which the items are shown.

Fig. 16.5-25 Data Portion Format

Item	No. of bytes	Description
Collision detection	1	00h: No collision, 01h: Collision, Other: Retained for future specification
No. of UID received	1	Number of UIDs normally received
Received UID1	8	First UID normally received
...	...	...
Received UIDn	8	nth UID normally received

If the status contents represented with SW1 and SW2 do not indicate normal termination, a data portion is not present in the response.

(d) Status

The status (SW1-SW2) values in the response of request all A are shown in "Table 16.5-26 Status".

Table 16.5-26 Status

SW1	SW2	Meaning
90	00	Normal termination
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (8) Select A

## (a) Operation

A SEL\_t command is sent to a type A PICC, and the received SAK\_t response is sent to an upper device.

(Refer to "12.5 Type A Timeslot - Initialization and Anticollision" for details regarding SEL\_t.)

When executing this command, the parameters are set to the type A time slot type and a communication speed of 106 kbps regardless of the PICC communication settings. Following execution of this command, the PICC communication settings return to their original settings.

## (b) Command Format

The command format of select A is shown in "Fig. 16.5-20 Command Format". Values represented in the form of xxh of each item in the figure indicate the encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA 00h	INS 23h	P1 CID	P2 00h	Lc	Data Proximity IC card UID
(1)	(1)	(1)	(1)	(1)	(Lc)

Fig. 16.5-20 Command Format

P1 is the same as that of CID in the SEL\_t command sent to the PICC.

The value of P2 is 00h, and other values are retained for future specification.

The value of Lc is the length of the data portion.

The data is the same as the UID in the SEL\_t command sent to the PICC.

## (c) Response Format

The response format of select A is shown in "Fig. 16.5-21 Response Format". Values in parentheses "( )" indicate the number of bytes.

Data	SW1	SW2
( )	(1)	(1)

Fig. 16.5-21 Response Format

The data portion is the SAK\_t response received from the PICC (excluding CRC).

If the status contents represented with SW1 and SW2 do not indicate normal termination, a data portion is not present in the response.

## (d) Status

The status (SW1-SW2) values in the response of Select A are shown in "Table 16.5-27 Status".

Table 16.5-27 Status

SW1	SW2	Meaning
90	00	Normal termination
62	F0	PICC communication receive timeout
62	F1	PICC communication receive error
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (9) Request for ATS

## (a) Operation

A RATS command is sent to a type A PICC, and the received ATS response is sent to an upper device.

(Refer to "13.1 Type A Protocol Activation" for details regarding RATS.)

When executing this command, the parameters are set to the type A time slot type and a communication speed of 106 kbps regardless of the PICC communication settings. Following execution of this command, the PICC communication settings return to their original settings.

## (b) Command Format

The command format of select A is shown in "Fig. 16.5-22 Command Format". Values represented in the form of xxh for each item in the figure indicate the encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA	INS	P1	P2
00h	25h	Param	00h
(1)	(1)	(1)	(1)

Fig. 16.5-22 Command Format

P1 is the same as that of Param portion in the RATS command sent to the PICC.  
The value of P2 is 00h, and other values are retained for future specification.

## (c) Response Format

The response format of ATS request is shown in "Fig. 16.5-23 Response Format". Values in parentheses "( )" indicate the number of bytes.

Data	SW1	SW2
()	(1)	(1)

Fig. 16.5-23 Response Format

The data portion is the ATS response received from the PICC (excluding CRC).

If the status contents represented with SW1 and SW2 do not indicate normal termination, a data portion is not present in the response.



## (d) Status

The status (SW1-SW2) values in the response of ATS request are shown in "Table 16.5-28 Status".

Table 16.5-28 Status

SW1	SW2	Meaning
90	00	Normal termination
62	F0	PICC communication receive timeout
62	F1	PICC communication receive error
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (10) Parameter Change

## (a) Operation

A PPS command is sent to a type A PICC, and the received response is sent to an upper device.

(Refer to "13.1 Type A Protocol Activation" for details regarding PPS.)

When executing this command, the parameters are set to the type A time slot type and a communication speed of 106 kbps regardless of the PICC communication settings. Following execution of this command, the PICC communication settings return to their original settings.

## (b) Command Format

The command format for parameter change is shown in "Fig. 16.5-24 Command Format". Values represented in the form of xxh for each item in the figure indicate the encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA	INS	P1	P2	Lc	Data
00h	27h	PPSS	00h		PPS0, PPS1
(1)	(1)	(1)	(1)	(1)	(Lc)

Fig. 16.5-24 Command Format

P1 is the same as of the PPSS in the PPS command sent to the PICC.

The value of P2 is 00h, and other values are retained for future specification.

The value of Lc is the length of the data portion.

The data are PPS0 and PPS1 in the PPS command sent to the PICC.

## (c) Response Format

The response format for parameter change is shown in "Fig. 16.5-25 Response Format". Values in parentheses "( )" indicate the number of bytes.

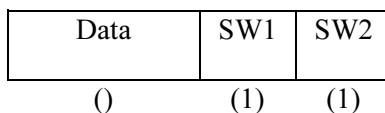


Fig. 16.5-25 Response Format

The data portion is the PPSS response received from the PICC (excluding CRC).

If the status contents represented with SW1 and SW2 do not indicate normal termination, a data portion is not present in the response.

## (d) Status

The status (SW1-SW2) values in the response for parameter change are shown in "Table 16.5-29 Status".

Table 16.5-29 Status

SW1	SW2	Meaning
90	00	Normal termination
62	F0	PICC communication receive timeout
62	F1	PICC communication receive error
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (11) Halt A

## (a) Operation

A HALT\_t command is sent to a type A PICC, and the received response is sent to an upper device. (Refer to "12.5 Type A Timeslot - Initialization and Anticollision" for details regarding HALT\_t.) When executing this command, the parameters are set to the type A time slot type and a communication speed of 106 kbps regardless of the PICC communication settings. Following execution of this command, the PICC communication settings return to their original settings.

## (b) Command Format

The command format of halt A is shown in "Fig. 16.5-26 Command Format". Values represented in the form of xxh for each item in the figure indicate the encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA 00h	INS 29h	P1 CID	P2 00h
(1)	(1)	(1)	(1)

Fig. 16.5-26 Command Format

P1 is the same as the CID of the destination PICC to which the HALT\_t command is sent. The value of P2 is 00h, and other values are retained for future specification.

## (c) Response Format

The response format of halt A is shown in "Fig. 16.5-27 Response Format". Values in parentheses "( )" indicate the number of bytes.

Data	SW1	SW2
()	(1)	(1)

Fig. 16.5-27 Response Format

The data portion is the response received from the PICC (excluding CRC). If the status contents represented with SW1 and SW2 do not indicate normal termination, a data portion is not present in the response.

## (d) Status

The status (SW1-SW2) values in the response of halt A are shown in "Table 16.5-30 Status".

Table 16.5-30 Status

SW1	SW2	Meaning
90	00	Normal termination
62	F0	PICC communication receive timeout
62	F1	PICC communication receive error
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (12) Request All B

## (a) Operation

An REQB command is sent to a type B PICC, and the PUPI, application data and protocol information in the ATQB response of the PICC normally received using a time slot are sent to an upper device.

(Refer to "12.2 Type B - Initialization and Anticollison" for details regarding REQB.)

When executing this command, the parameters are set to the type B time slot type and a communication speed of 106 kbps regardless of the PICC communication settings. Following execution of this command, the PICC communication settings return to their original settings.

## (b) Command Format

The command format of request all B is shown in "Fig. 16.5-28 Command Format". Values represented in the form of xxh for each item in the figure indicate the encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA	INS	P1	P2
00h	31h	AFI	Param
(1)	(1)	(1)	(1)

Fig. 16.5-28 Command Format

P1 is the same as the AFI in the REQB command sent to the PICC.

P2 is the same as the Param in the REQB command sent to the PICC.

## (c) Response Format

The response format of request all B is shown in "Fig. 16.5-29 Response Format". Values in parentheses "( )" indicate the number of bytes.

Data	SW1	SW2
( )	(1)	(1)

Fig. 16.5-29 Response Format

The format of the data portion is shown in "Table 16.5-31 Data Portion Format".

Table 16.5-31 Data Portion Format

Item	No. of bytes	Description
Collision detection	1	00h: No collision, 01h: Collision, Other: Retained for future specification
No. of information received	1	Number of PICC of which the ATQB was normally received
Received information 1	11	First normally received information (PUP1, application data, protocol information)
...	...	...
Received information n	11	nth normally received information (PUP1, application data, protocol information)

If the status contents represented with SW1 and SW2 do not indicate normal termination, a data portion is not present in the response.

## (d) Status

The status (SW1-SW2) values in the response of request all B are shown in "Table 16.5-32 Status".

Table 16.5-32 Status

SW1	SW2	Meaning
90	00	Normal termination
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (13) Attribute

## (a) Operation

A ATTRIB command is sent to a type B PICC, and the received response is sent to an upper device.

(Refer to "12.2 Type B Initialization and Anticollision" for details regarding ATTRIB.)

When executing this command, the parameters are set to the type B time slot type and a communication speed of 106 kbps regardless of the PICC communication settings. Following execution of this command, the PICC communication settings return to their original settings.

## (b) Command Format

The command format of attribute is shown in "Fig. 16.5-30 Command Format". Values represented in the form of xxh for each item in the figure indicate the encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA 00h	INS 33h	P1 00h	P2 00h	Lc	Data ATTRIB
(1)	(1)	(1)	(1)	(1)	(Lc)

Fig. 16.5-30 Command Format

P1 and P2 are each fixed at 00h, and other values are retained for future specification.

Lc is the length of the data portion.

The data portion consists of the Identifier, Param 1, Param 2, Param 3, CID and Higher Layer INF in the ATTRIB command sent to the PICC.



## (c) Response Format

The response format of attribute is shown in "Fig. 16.5-31 Response Format". Values in parentheses "( )" indicate the number of bytes.

Data	SW1	SW2
( )	(1)	(1)

Fig. 16.5-31 Response Format

The data portion is the response received from the PICC (excluding CRC).

If the status contents represented with SW1 and SW2 do not indicate normal termination, a data portion is not present in the response.

## (d) Status

The status (SW1-SW2) values in the response of attribute are shown in "Table 16.5-33 Status".

Table 16.5-33 Status

SW1	SW2	Meaning
90	00	Normal termination
62	F0	PICC communication receive timeout
62	F1	PICC communication receive error
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (14) Halt B

## (a) Operation

A HLTB command is sent to a type B PICC, and the received response is sent to an upper device. (Refer to "12.2 Type B Initialization and Anticollision" for details regarding HLTB.)

When executing this command, the parameters are set to the type B time slot type and a communication speed of 106 kbps regardless of the PICC communication settings. Following execution of this command, the PICC communication settings return to their original settings.

## (b) Command Format

The command format of halt B is shown in "Fig. 16.5-32 Command Format". Values represented in the form of xxh for each item in the figure indicate the encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA	INS	P1	P2	Lc	Data Identifier
00h	39h	00h	00h		
(1)	(1)	(1)	(1)	(1)	(Lc)

Fig. 16.5-32 Command Format

P1 and P2 are each fixed at 00h, and other values are retained for future specification.

Lc is the length of the data portion.

The data portion is the Identifier in the HLTB command sent to the PICC.

## (c) Response Format

The response format of halt B is shown in "Fig. 16.5-33 Response Format". Values in parentheses "( )" indicate the number of bytes.

Data	SW1	SW2
( )	(1)	(1)

Fig. 16.5-33 Response Format

The data portion is the response received from the PICC (and does not contain CRC).

If the status contents represented with SW1 and SW2 do not indicate normal termination, a data portion is not present in the response.

## (d) Status

The status (SW1-SW2) values in the response of halt B are shown in "Table 16.5-34 Status".

Table 16.5-34 Status

SW1	SW2	Meaning
90	00	Normal termination
62	F0	PICC communication receive timeout
62	F1	PICC communication receive error
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (15) Wake-up All B

## (a) Operation

An WUPB command is sent to a type B PICC, and the PUPI, application data and protocol information in the ATQB response of the PICC normally received using a time slot are sent to an upper device.

(Refer to "12.2 Type B Initialization and Anticollision" for details regarding WUPB.)

When executing this command, the parameters are set to the type B time slot type and a communication speed of 106 kbps regardless of the PICC communication settings. Following execution of this command, the PICC communication settings return to their original settings.

## (b) Command Format

The command format of wake-up all B is shown in "Fig. 16.5-34 Command Format". Values represented in the form of xxh for each item in the figure indicate the encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA	INS	P1	P2
00h	3Bh	AFI	Param
(1)	(1)	(1)	(1)

Fig. 16.5-34 Command Format

P1 is the same as the AFI in the WUPB command sent to the PICC.

P2 is the same as the Param in the WUPB command sent to the PICC.

## (c) Response Format

The response format of wake-up all B is shown in "Fig. 16.5-35 Response Format". Values in parentheses "( )" indicate the number of bytes.

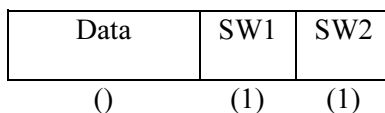


Fig. 16.5-35 Response Format

The format of the data portion is shown in "Table 16.5-35 Data Portion Format".

Table 16.5-35 Data Portion Format

Item	No. of bytes	Description
Collision detection	1	00h: No collision, 01h: Collision, Other: Retained for future specification
No. of information received	1	Number of PICC of which the ATQB was normally received
Received information 1	11	First normally received information (PUPI, application data, protocol information)
...	...	...
Received information n	11	nth normally received information (PUPI, application data, protocol information)

If the status contents represented with SW1 and SW2 do not indicate normal termination, a data portion is not present in the response.

## (d) Status

The status (SW1-SW2) values in the response of wake-up all B are shown in "Table 16.5-36 Status".

Table 16.5-36 Status

SW1	SW2	Meaning
90	00	Normal termination
64	00	Execution error
67	00	Command length error
6B	00	P1, P2 error

## (16) PCD Self-Diagnosis

## (a) Operation

Self-diagnosis of the PCD is performed.

Items eligible for self-diagnosis are shown in "Table 16.5-37 Self-Diagnosis Items".

Table 16.5-37 Self-Diagnosis Items

Item	P1-P2	Description
Modulation data "0" output	0000h	Data modulated with data "0" is continuously output.
Modulation data "1" output	0001h	Data modulated with data "1" is continuously output.
Modulation data random output	0002h	Data modulated randomly is continuously output.

## (b) Command Format

The command format of PCD self-diagnosis is shown in "Fig. 16.5-36 Command Format". Values represented in the form of xxh for each item in the figure indicate the encoding of that item, while values in parentheses "( )" indicate the number of bytes.

CLA 00h	INS F1h	P1	P2
(1)	(1)	(1)	(1)

Fig. 16.5-36 Command Format

The values of P1 and P2 are as shown in "Table 16.5-37 Self-Diagnosis Items". Other values of P1 and P2 are retained for future specification.

## (c) Response Format

The PCD does not return a response when this command is executed.

### 16.6Reference Information

The communication sequence between an upper device and PCD is described here as reference information. In addition, communication between the PCD and PICC is also described as necessary.

#### 16.6.1 Normal Communication Sequence Examples

Example of normal communication sequences are shown below.

##### (1) PCD Initialization

The sequence through initialization of the PCD and enabling of communication with the PICC is shown in "Fig. 16.6-1 Initialization Sequence".

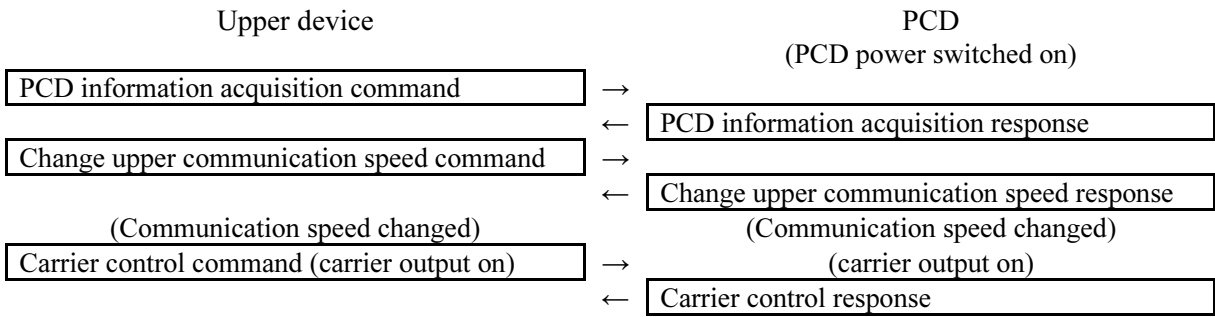


Fig. 16.6-1 Initialization Sequence

## (2) Type B PICC Detection (One Card)

The sequence for detecting a type B PICC where initialization of the PCD has been completed is shown in "Fig. 16.6-2 Type B PICC Detection Sequence 1" (case of one PICC).

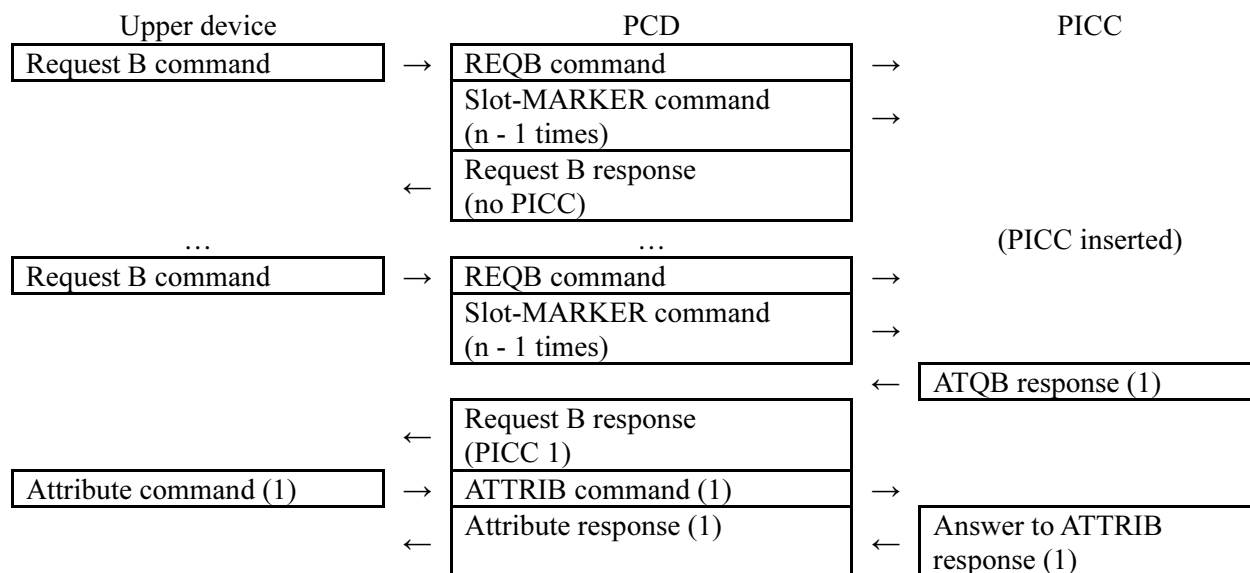


Fig. 16.6-2 Type B PICC Detection Sequence 1

The numbers in parentheses are the number of the PICC for the sake of convenience, and indicate that the information of the corresponding card is sent.



## (3) Type B PICC Detection (Multiple Cards)

The sequence for detecting a type B PICC where initialization of the PCD has been completed is shown in "Fig. 16.6-3 Type B PICC Detection Sequence 2" (case of two PICC).

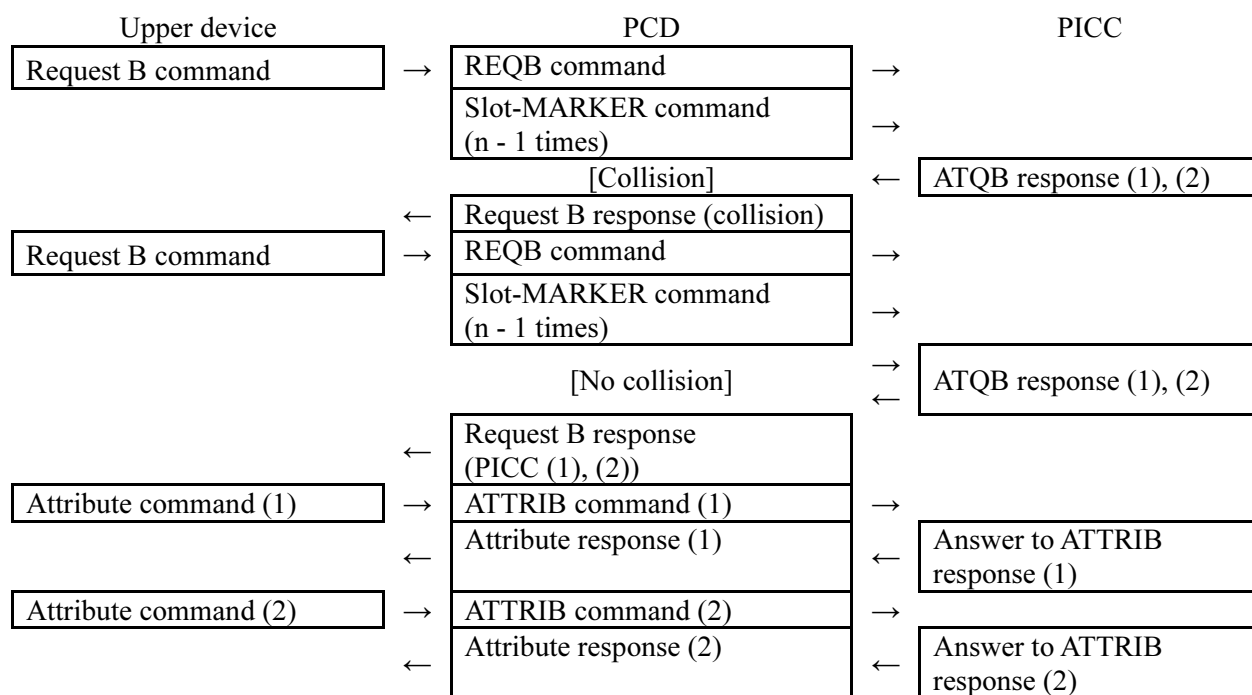


Fig. 16.6-3 Type B PICC Detection Sequence 2

The numbers in parentheses are the number of the PICC for the sake of convenience, and indicate that the information of the corresponding card is sent.

## (4) Type A PICC Detection (Multiple Cards)

The sequence for detecting a type A PICC where initialization of the PCD has been completed is shown in "Fig. 16.6-4 Type A PICC Detection Sequence" (case of two PICC).

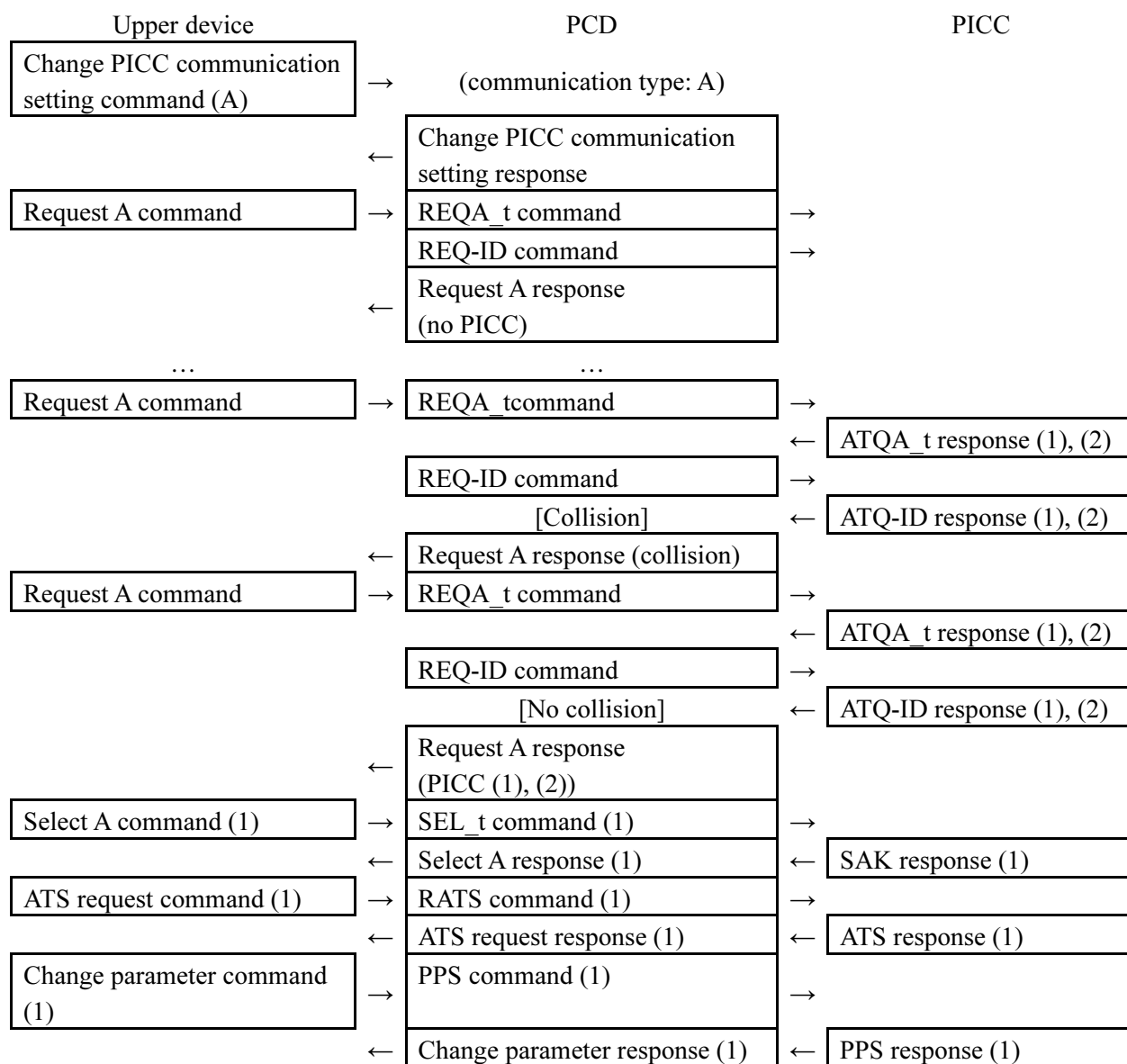


Fig. 16.6-4 Type A PICC Detection Sequence

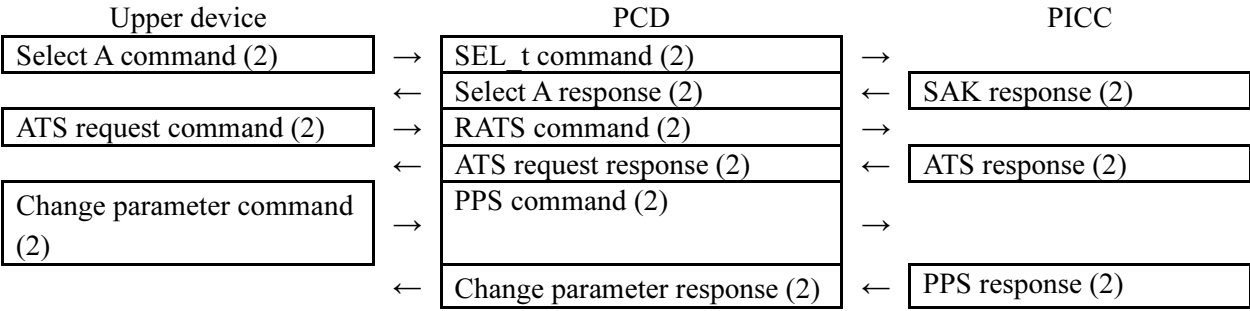


Fig. 16.6-4 Type A PICC Detection Sequence (continued)

The numbers in parentheses are the number of the PICC for the sake of convenience, and indicate that the information of the corresponding card is sent.

(5) PICC Deactivation

The sequence for deactivating a PICC where detection of the PICC has been completed is shown in "Fig. 16.6-5 PICC Deactivation Sequence 5".

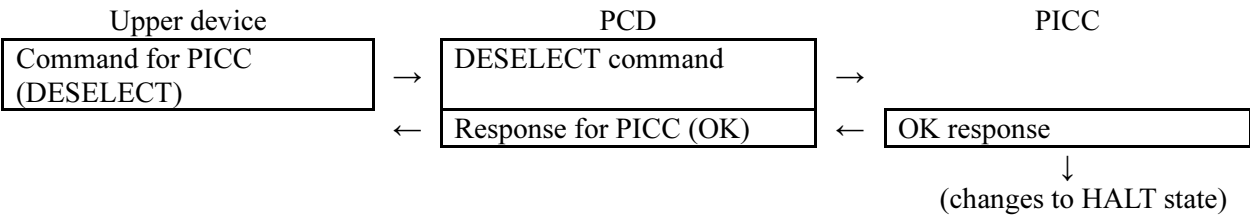


Fig. 16.6-5 PICC Deactivation Sequence 5

## 16.6.2 Abnormal Communication Sequence Example

The following indicates communication sequences on event of an error.

### (1) PCD Receive Error

The processing sequence when the PCD has judged a command received from an upper device to be a receive error is shown in "Fig. 16.6-6 PCD Receive Error Sequence".

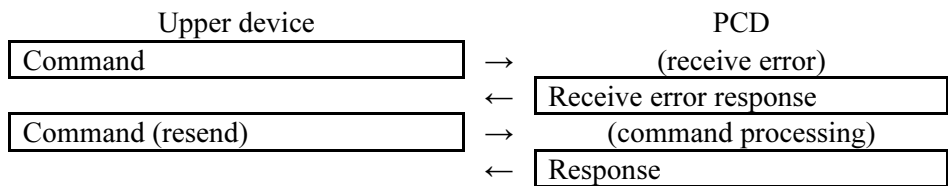


Fig. 16.6-6 PCD Receive Error Sequence

### (2) Upper Device Receive Error

The processing sequence when an upper device has judged a response received from the PCD to be a receive error is shown in "Fig. 16.6-7 Upper Device Receive Error Sequence".

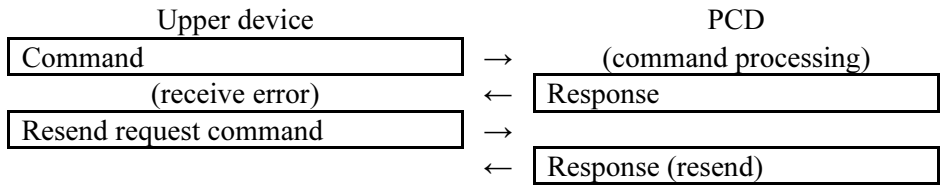


Fig. 16.6-7 Upper Device Receive Error Sequence

### (3) Upper Communication Speed Change Error 1

The processing sequence when an upper device has judged a response received from the PCD to be a receive error during a change upper communication speed command is shown in "Fig. 16.6-8 Upper Communication Speed Change Error Sequence 1".

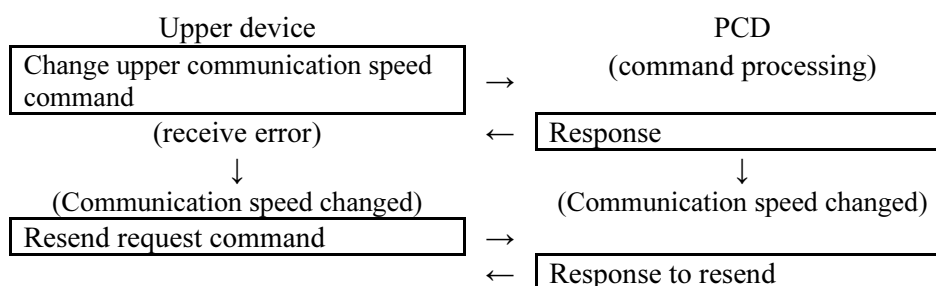


Fig. 16.6-8 Upper Communication Speed Change Error Sequence 1

If the upper device receives any response, it considers the PCD has performed processing normally and changes the communication speed.

## (4) Upper Communication Speed Change Error 2

The processing sequence when the PCD has judged a command received from an upper device to be a receive error during a change upper communication speed command, and the upper device has judged a response received from the PCD to be a receive error is shown in "Fig. 16.6-9 Upper Communication Speed Change Error Sequence 2".

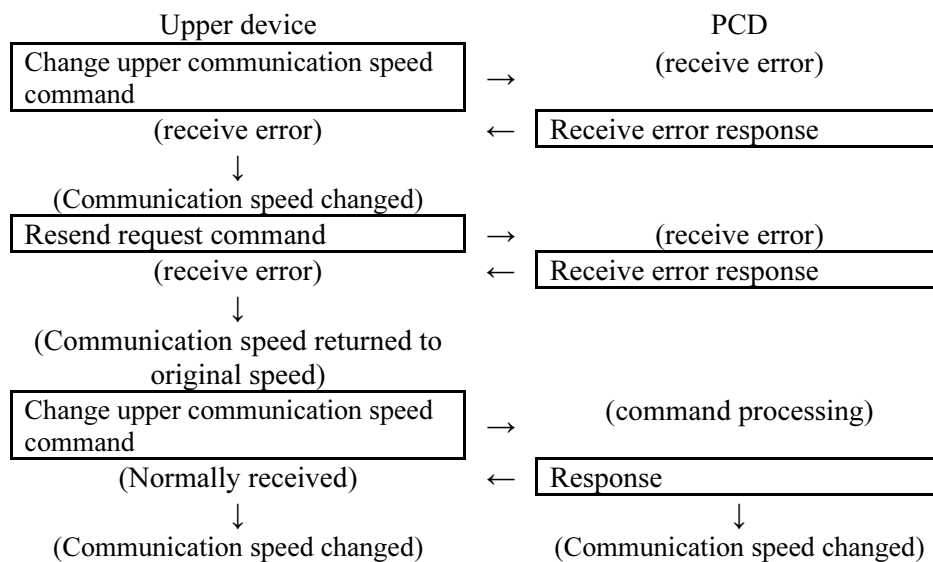


Fig. 16.6-9 Upper Communication Speed Change Error Sequence 2

If the upper device receives any response, it considers the PCD has performed processing normally and changes the communication speed. If a receive error occurs again when sending a request in response to the resend command, the communication speed returns to its original speed.

(5) PICC Communication Error 1

The processing sequence where the PCD has judged a response received from a PICC to be a receive error during a command for the PICC is shown in "Fig. 16.6-10 PICC Communication Error Sequence 1".

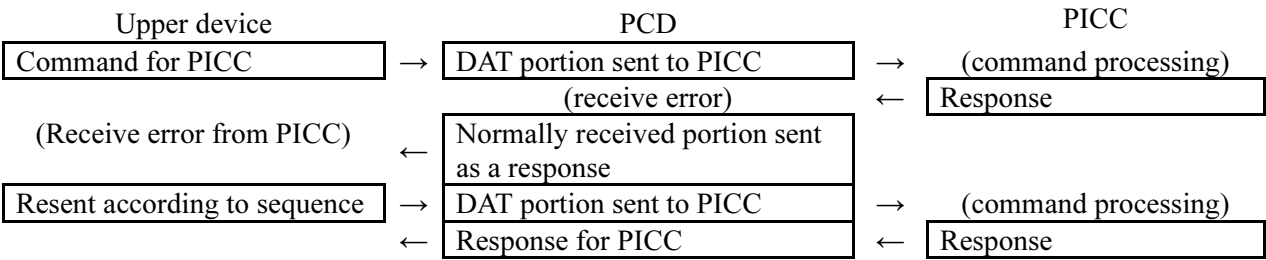


Fig. 16.6-10 PICC Communication Error Sequence 1

If the upper device has judged there was a receive error from the PICC, the command is resent according to the transmission sequence of the PICC.

## (6) PICC Communication Error 2

The processing sequence where an upper device has judged that a timeout has occurred waiting for a response from the PCD during a command for the PICC (caused by a receive error in the PICC) is shown in "Fig. 16.6-11 PICC Communication Error Sequence 2".

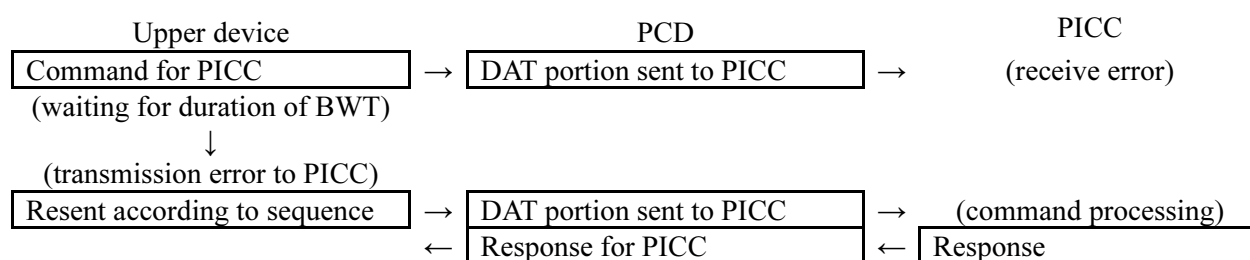


Fig. 16.6-11 PICC Communication Error Sequence 2

If the upper device has judged there is no response from the PICC, the command is resent according to the transmission sequence of the PICC.



## (7) PICC Communication Error 3

The processing sequence where an upper device has judged that a timeout has occurred waiting for response from the PCD during a command for the PICC (caused by absence of the PICC) is shown in "Fig. 16.6-12 PICC Communication Error Sequence 3".

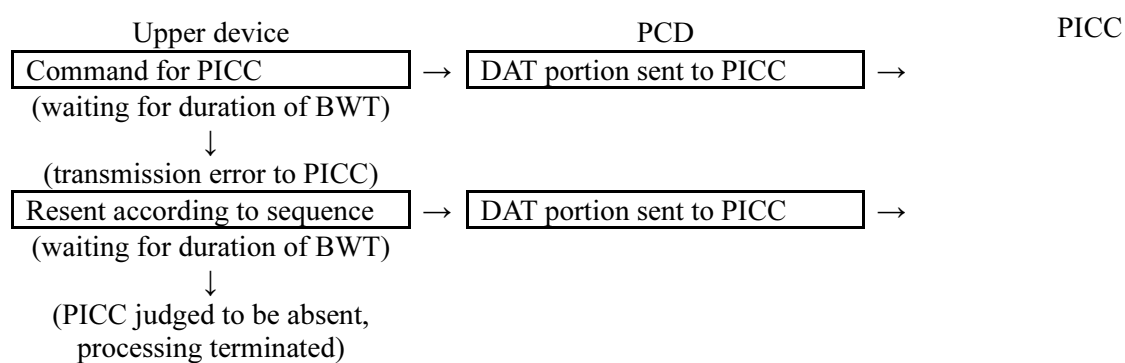


Fig. 16.6-12 PICC Communication Error Sequence 3

If the upper device has judged there is no response from the PICC and there is no response even after resending, it is judged to be absent according to the transmission sequence of the PICC.

## 17. Compatibility Test Method

The test method is specified for evaluating interoperability and compatibility of a PICC and PCD. In addition, the contents of evaluation by cross-testing the PICC and PCD are also specified.

### (1) Verification Levels

Verification levels are shown in "Table 17-1 Compatibility Test Levels".

Table 17-1 Compatibility Test Levels

No	Verification level	Verified contents	Evaluation
1	Signal level	Send commands from the PCD and monitor the response from the card at the receive signal level of the PCD based on "9. Communication PCD to PICC" and "10. Communication PICC to PCD".	Evaluated as being compatible if the response from the card is at a level that can be received with the PCD.
2	Polling	Verify the response from the card in response to an REQ command from the PCD based on "11. Polling".	Evaluated as being compatible if the response from the card can be received with the PCD.
3	Anticollision	Detect one or two cards based on "12. Anticollision".	Evaluated as being compatible if the PCD is able to recognize all cards.
4	Transmission protocol	Send command from the PCD to the card, and verify the response from the card based on "13. Transmission Protocol".	Evaluated as being compatible if the response from the card complies with the specifications.

## (2) Test Combinations

Test combinations are shown in "Fig. 17-1 Block Diagram". Which combination of tests to be performed is selected according to the functions of the equipment being tested.

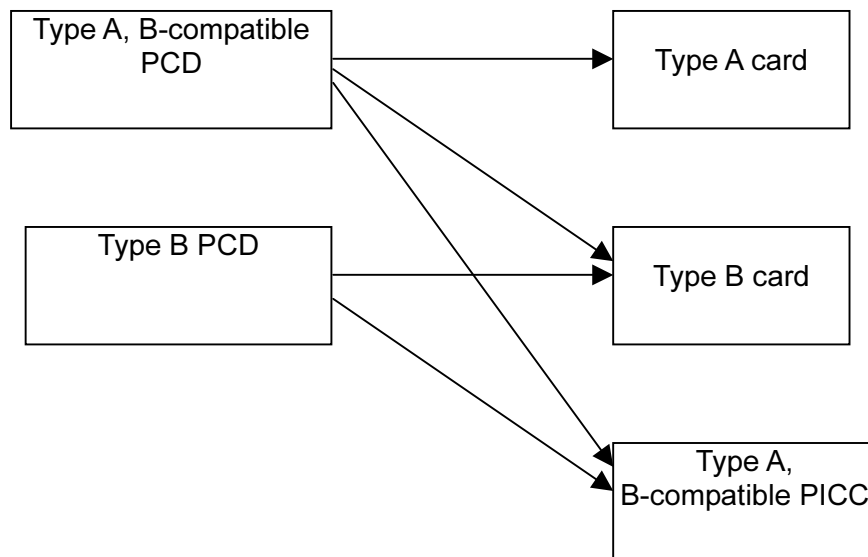


Fig. 17-1 Block Diagram

## [Reference] Example of Compatibility Verification Sheet

Card

Note: For the purpose of distinction, the reference PICC of the basic specifications is designated as reference PICC-M, while the calibration coil is designated as calibration coil-M.

Item	Measuring conditions		Specifications	Classification			Card type		Measurement results	Evaluation	Remarks
				Basic	Extended	Reference	For single card operation	For two card operation			
14.3.1.2 Minimum Operating Magnetic Field Test	Single card		1.5 A/m or less	√							
			(4) A/m or less		√						
	Superimposed cards	Two cards	(4) A/m or less		√		(not applicable)				
		Ref. PICC-M	(4) A/m or less		√		(not applicable)				
		Ref. PICC-S	(4) A/m or less		√		(not applicable)				
		Ref. PICC-L	(4) A/m or less		√		(not applicable)				
14.3.1.3 Maximum Operating Magnetic Field Test	Single card		7.5 A/m or more	√							
	Superimposed cards	Two cards	7.5 A/m or more		√		(not applicable)				
		Ref. PICC-M	7.5 A/m or more		√		(not applicable)				
		Ref. PICC-S	7.5 A/m or more		√		(not applicable)				
		Ref. PICC-L	7.5 A/m or more		√		(not applicable)				
14.3.1.4 Maximum Applied Magnetic Field Test	Single card		Card must function normally after applying magnetic field		√						
	Superimposed cards	Two cards	Card must function normally after applying magnetic field		√		(not applicable)				
		Ref. PICC-M	Card must function normally after applying magnetic field		√		(not applicable)				
		Ref. PICC-S	Card must function normally after applying magnetic field		√		(not applicable)				
		Ref. PICC-L	Card must function normally after applying magnetic field		√		(not applicable)				
14.3.1.5 Signal Receive Test	Single card		Must be able to receive		√						
14.3.1.6 Load Modulation Test	Single card		Modulation level: 30/H ^ 1.2 mVp or more	√							
	Superimposed cards	Two cards	Modulation level: 30/H ^ 1.2 mVp or more		√		(not applicable)				
		Ref. PICC-M	Modulation level: 30/H ^ 1.2 mVp or more		√		(not applicable)				
		Ref. PICC-S	Modulation level: 30/H ^ 1.2 mVp or more		√		(not applicable)				
		Ref. PICC-L	Modulation level: 30/H ^ 1.2 mVp or more		√		(not applicable)				
14.3.1.7 Reference PICC Superimposition Test	Superimposed cards	Ref. PICC-M	Receive voltage of (6.8) V or more at load of 910 Ohm		√		(not applicable)				
		Ref. PICC-S	Receive voltage of (6.8) V or more at load of 910 Ohm		√		(not applicable)				
		Ref. PICC-L	Receive voltage of (6.8) V or more at load of 910 Ohm		√		(not applicable)				
14.3.2 Testing Using Test PCD-S	Single card		Must receive response from card			√					
	Superimposed cards	Two cards	Must receive response from card			√					
		Ref. PICC-M	Must receive response from card			√					
		Ref. PICC-S	Must receive response from card			√					
		Ref. PICC-L	Must receive response from card			√					

## PCD

Item		Measuring conditions		Specifications		Classification			RW type		Measurement results	Evaluation	Remarks
						Basic	Extended	Reference	Slot insertion	Open			
15.3.1	Magnetic Field Strength	Maximum Generated Magnetic Field	Reference PICC used	Ref. PICC-M	3V or less	√							
				Ref. PICC- S	Same as above		√						
				Ref. PICC- L	Same as above		√						
	Minimum Generated Magnetic Field	↑		Ref. PICC-M	3V (1.5A/m) or more	√							
					3V (4A/m) or more		√						
				Ref. PICC- S	Same as above		√						
				Ref. PICC- L	Same as above		√						
15.3.2	Power Transfer Test	One reference PICC (resonance frequency: 19 MHz)		Calibration coil used	Calibration coil-M	7.5A/m or less		√					
				Minimum Generated Magnetic Field	Calibration coil used	Calibration coil-M	(4)A/m or more		√				
				Ref. PICC-M	3 V or more at load of 8 kOhm	√							
				Ref. PICC-M	(6.8) V or more at load of 910Ohm			√					
		Two reference PICCs		Ref. PICC- S	(6.8) V or more at load of 910Ohm			√					
				Ref. PICC- L	(6.8) V or more at load of 910Ohm			√					
				M-M	(6.8) V or more at load of 910Ohm			√		(not applicable)			
				M-S	(6.8) V or more at load of 910Ohm			√		(not applicable)			
				M-L	(6.8) V or more at load of 910Ohm			√		(not applicable)			
				S-M	(6.8) V or more at load of 910Ohm			√		(not applicable)			
				S-S	(6.8) V or more at load of 910Ohm			√		(not applicable)			
				S-L	(6.8) V or more at load of 910Ohm			√		(not applicable)			
				L-M	(6.8) V or more at load of 910Ohm			√		(not applicable)			
				L-S	(6.8) V or more at load of 910Ohm			√		(not applicable)			
				L-L	(6.8) V or more at load of 910Ohm			√		(not applicable)			
15.3.3	Modulation Waveform	Calibration coil used		Calibration coil-M	Specifications must be satisfied	√							
				One reference PICC	Ref. PICC-M		√						
				Ref. PICC- S	Same as above		√						
				Ref. PICC- L	Same as above		√						
		Two reference PICCs		M-M	Same as above		√			(not applicable)			
				M-S	Same as above		√			(not applicable)			
				M-L	Same as above		√			(not applicable)			
				S-M	Same as above		√			(not applicable)			
				S-S	Same as above		√			(not applicable)			
				S-L	Same as above		√			(not applicable)			
				L-M	Same as above		√			(not applicable)			
				L-S	Same as above		√			(not applicable)			
15.3.4	Reception Ability of Load Modulation Signal			Ref. PICC-M	Must be able to receive	√							
				Ref. PICC- S	Same as above		√						
				Ref. PICC- L	Same as above		√						